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NOTES:
1. HSF Property: Comply iSupplier system HSF property attribute up-to-date value.

Eletro-XTechnical

LOCATION	LEVEL	U42	U22
PAD6015	PVBAT	SHORT	SHORT
PAD6020	P5V0A	SHORT	SHORT
PAD60210	PVBAT	SHORT	SHORT
PAD60100	P3V3A	SHORT	SHORT
PAD60110	PVBAT	SHORT	SHORT
PAD60103	P3V3AL	SHORT	SHORT
PAD60310	PVBAT	SHORT	SHORT
PAD60300	P1V2	SHORT	SHORT
PAD60350	P0V6S	SHORT	SHORT
PAD60600	P1V8A	SHORT	SHORT
PAD60610	P3V3A	SHORT	SHORT
PAD60800	P1V0A	SHORT	SHORT
PAD60810	PVBAT	SHORT	SHORT
PAD66020	PVBAT	SHORT	OPEN
PAD66010	PVBAT	SHORT	SHORT
PAD66301	PVBAT	SHORT	SHORT
PAD66610	PVBAT	SHORT	SHORT
PAD60400	P2V5	SHORT	SHORT
PAD60410	P3V3A	SHORT	SHORT
PAD4500	PVCORE	SHORT	OPEN
PAD4501	PVCCGT	OPEN	SHORT
PAD4502	PVCORE	SHORT	OPEN
PAD1910	P3V3S	SHORT	SHORT
PAD1300	P3V3S	SHORT	SHORT
PAD500	AGND	SHORT	SHORT
PAD67010	PVBAT	SHORT	SHORT
PAD67200	P1V5S_DGPU	SHORT	SHORT
PAD67210	PVBAT	SHORT	SHORT
PAD67500	PVPCIIE	SHORT	SHORT
PAD67510	P3V3A	SHORT	SHORT
PAD7000	P3V3S	SHORT	SHORT

CPU LIST				
I3-7020U(N)	H-0 STEPPING	KBL-U22	6025B0343101	QNZU
I3-8130U	Y-0 STEPPING	KBL-R42	6025B0343301	QP8K
I3-7020U(F)	Y-0 STEPPING	KBL-R42	6025B0343001	QN96
I5-8250U	Y-0 STEPPING	KBL-R42	6025B0335901	SR3LA
I7-8550U	Y-0 STEPPING	KBL-R42	6025B0335801	SR3LC

GPU LIST			
AMD R17M-M1-30	GDDR5 216-0890010		6019B1639401
AMD R17M-M1-70	GDDR5 216-0889018		6019B1639501

VRAM LIST		
Hynix	H5GC8H24MJR-R0C	6019B1542101
Micron	MT51J256M32HF-70-A	6019B1486001
Samsung	K4G80325FB-HC28	6019B1485901

GRANGER 1.0
INTEL CORE 2 DUO LAK E - U
DIS : 25W 3X23
GPU : AMD M1-30/70
VRAM : GDDR5 512MX16
MV BUILD
2018.03.12

ID PIN FOR BIOS

PROJECT_ID	R42 15W	U22 15W
R4579	MOUNT	OPEN
R4578	OPEN	MOUNT
	3V	0V

BOARD_ID2	M1-70	M1-30
R4599	MOUNT	OPEN
R4618	OPEN	MOUNT
	3V	0V

DGPU_PSWRTR	UMA	DIS
R4589	MOUNT	OPEN
R4590	OPEN	MOUNT
	3V	0V

DGPU_PSWRTR	UMA	DIS
R4591	MOUNT	OPEN

BOARD_ID0	17"	14"
R4632	MOUNT	OPEN
R4514	OPEN	MOUNT
	3V	0V

BUILD_ID	ID1 17"	ID0 14"
DB	0	0
SI	0	1
PV	1	0
MV	1	1

BOARD_ID1	VRAMP4	VRAMP2
R4535	MOUNT	OPEN
R4536	OPEN	MOUNT
	3V	0V

ID PIN FOR EC

GPU_UMA_SEL	DIS	UMA
R392	MOUNT	OPEN
R393	OPEN	MOUNT
	3V	0V

Phase_ID	SI	DB	PV / MV
R337	10K_short	10K_short	10K_short
R322	10K_short	10K_short	10K_short
	3V	1.5V	0V

GPU_ID	M1-70	M1-30
R390	MOUNT	OPEN
R391	OPEN	MOUNT
	3V	0V

EC_PROJECT_ID	SNAP17	GRANGER14
R310	10K_short	10K_short
R311	10K_short	10K_short
	3V	0V

ADP_SEL	65W	45W
R307	MOUNT	OPEN
R309	OPEN	MOUNT
	3V	0V

CPU_ID	R42 15W	U22 15W
R343	MOUNT	OPEN
R338	OPEN	MOUNT
	3V	0V

R17M-M1-30/70 SVI2 LEVEL SHIFT OPTION TABLE

R17M-M1 30(3.3V)
R17M-M1 70(1.8V)

ATI_R17	R5216	R5217	R5220	R5219	R5218	R5225	R5226	R5221
M1-70	DY	DY	DY	DY	DY	DY	DY	DY
M1-30	STUFF	STUFF	DY	STUFF	STUFF	STUFF	STUFF	DY

R17M-M1-30/70 VR SETTING

NOTE: WHEN TSEN OR TSEN_NB IS LESS THEN 2.2V THE VRHOT_L WILL BE PULLED LOW.

ATI_R17	TDC (A)	EDC(A)	OCF (A)	LOAD LINE	R67038	R67039	R67040	R67022	R67024
M1-70	28	42	60	1 MOHM	71.5K	12.4K	0 OHM	DY	2.2 OHM
M1-30	28	42	60	0 MOHM	26.7K	17.4K	243 OHM	2.2 OHM	DY

R17M-M1-30/70 SVI2 OPTION TABLE

ATI_R17	R5100	R5101	R5102	R5103	R5104	R5105
M1-70	DY	DY	10K	DY	10K	DY
M1-30	DY	DY	DY	DY	DY	DY

R17M-M1-30/70 LOAD LINE OPTION TABLE

ATI_R17	R5213	R5212
M1-70	0 OHM	0 OHM
M1-30	DY	DY

R17M-M1-30/70 VCORE POWER OPTION TABLE

ATI_R17	R5202	R5206
M1-70	0 OHM	0 OHM
M1-30	DY	DY

R17M-M1-30/70 MLPS OPTION TABLE

ATI_R17	R5051	R5050
M1-70	DY	DY
M1-30	DY	STUFF

R17M-M1-30/70 PART NUMBER TABLE

ATI_R17	U5000
M1-70	6019B1639501
M1-30	6019B1639401

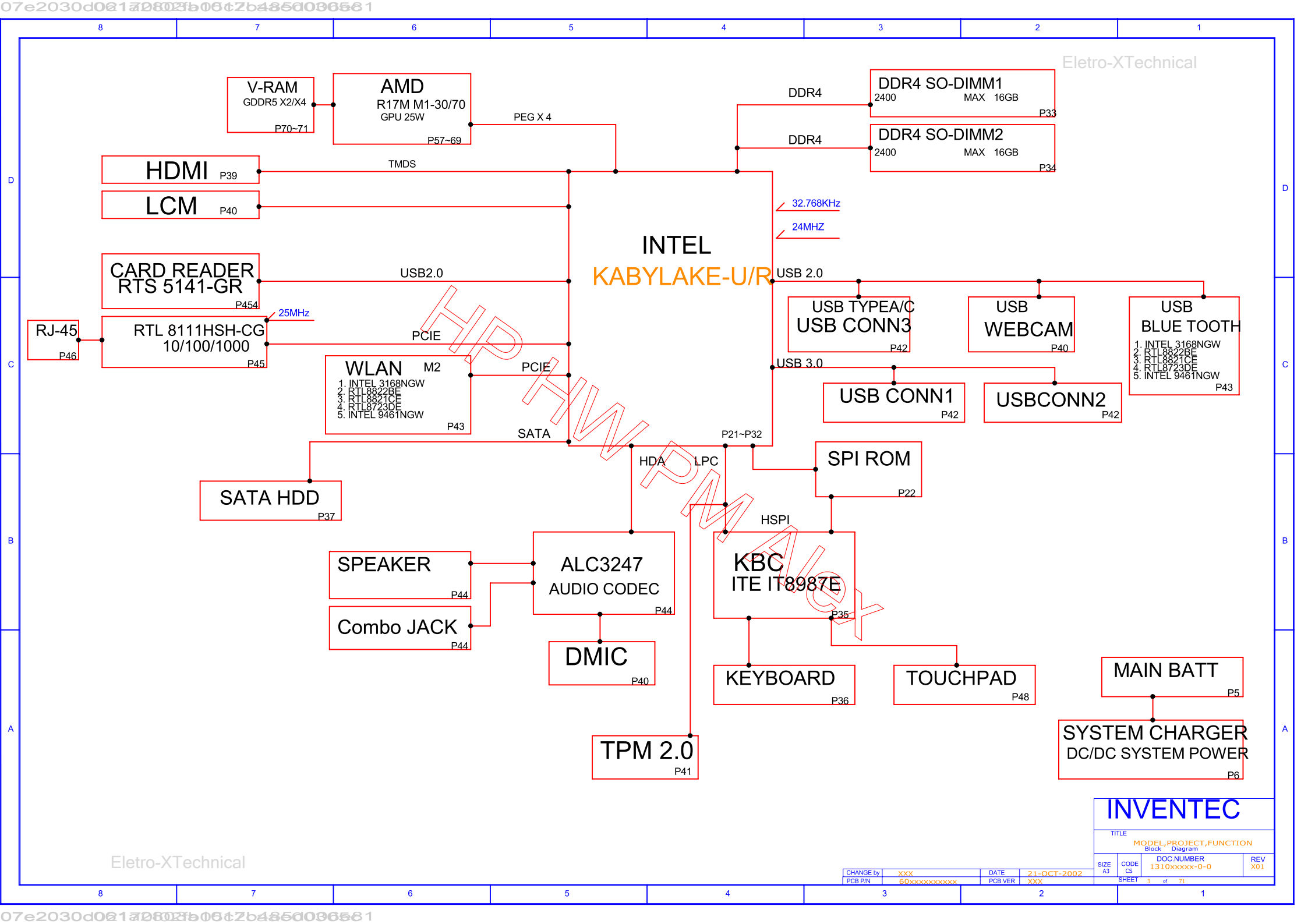
Eletro-XTechnical

DATE	CHANGE NO.	REV
24-OCT-2002		

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK	XXX		
APPROVAL	XXX		
FILE NAME	MLB 17" - RANGERS		
PCB FN	60XXXXXXX		

SIZE	A3	CODE	CS
SHEET	1		

INVENTEC			
MLB 17" - RANGERS		Main Board	
DOC NUMBER	1.31.0XXXXX-U-0	REV	X01



INVENTEC

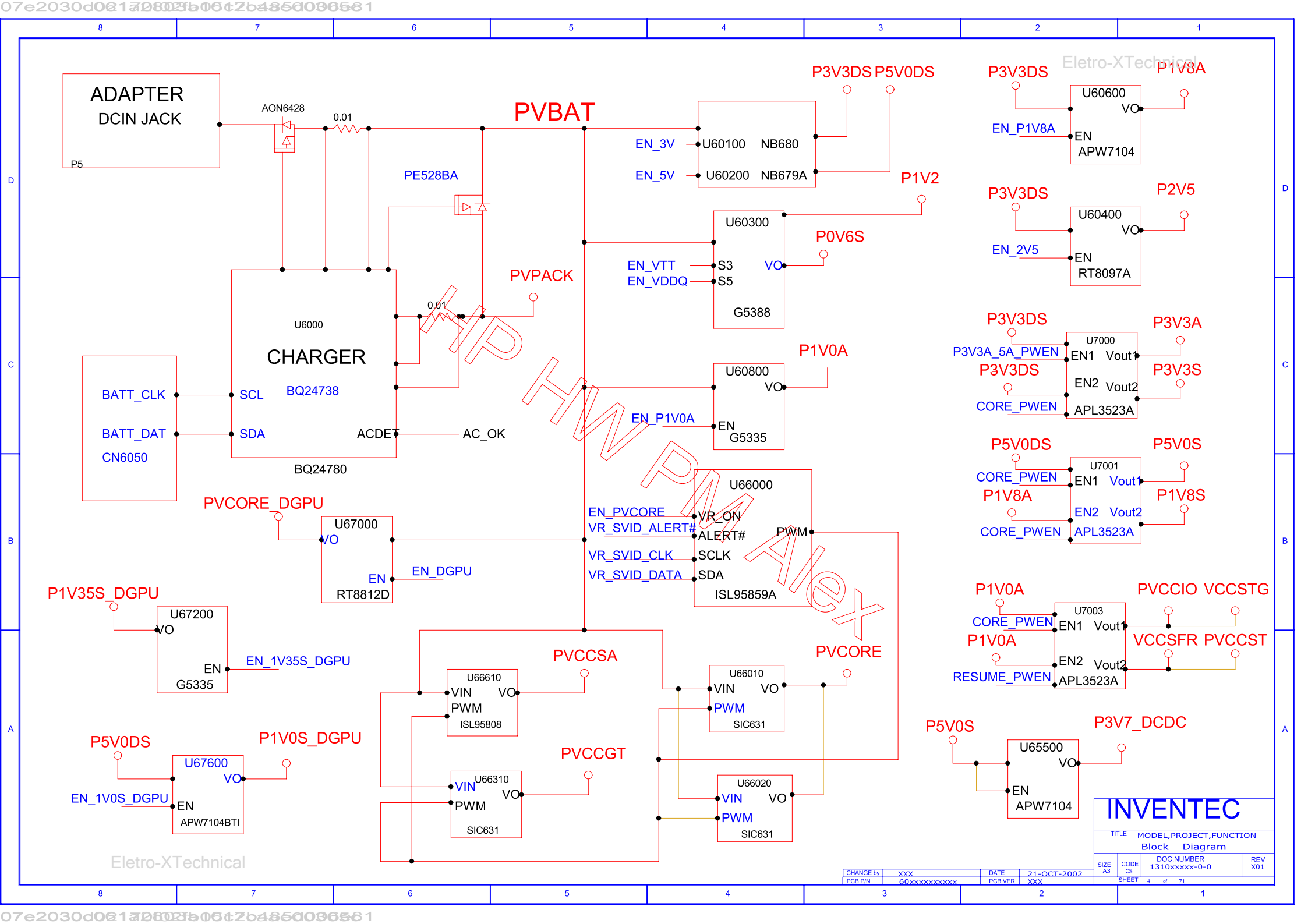
TITLE MODEL, PROJECT, FUNCTION

Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

SHEET 3 of 71

CHANGE by XXX DATE 21-OCT-2002 PCB P/N 60xxxxxxxxx PCB VER XXX



INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	
SHEET 4	of 71	REV X01	

CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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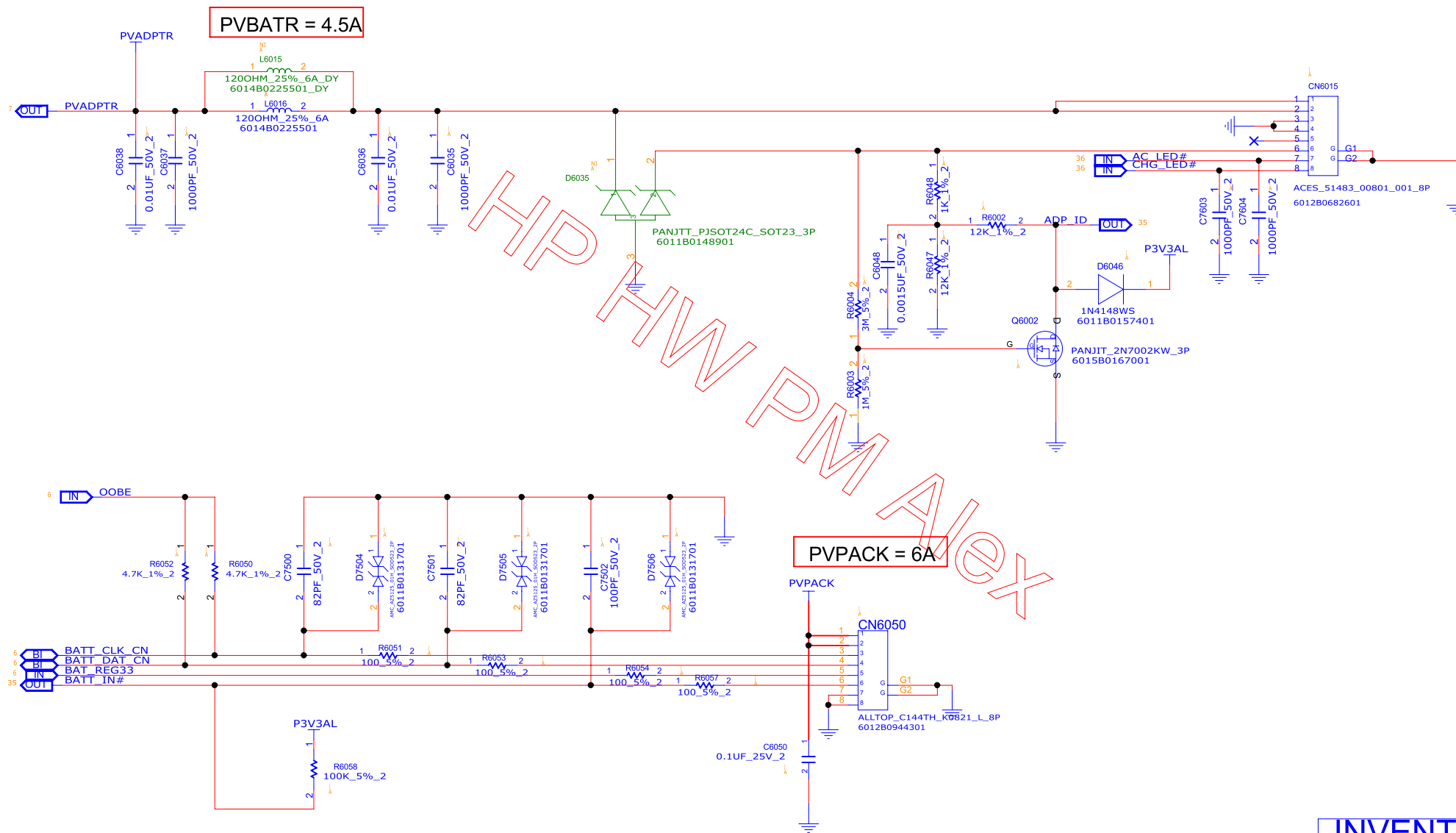
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11 P1V8A_APW7104	45 LAN_RTL8111HSH	
12 P1V0A(G5335)	46 TRANSFORMER & RJ45	
13 VCORE>&SA CONTROLLER_RT3602A	47 EMC CAP	
14 VCORE_SIC634	48 MB TO DB CONN & SCREW	
15 VCCGT_SIC534	49 MB TO CR USB BOARD	
16 VCCSA_RT9610C-AON7934	50 DB COVER	
17 P2V5_RT8097	51 NAB_USB3.0	
18 POWER LOAD SW	52 NAB_USB3.0 HUB	
19 ENABLE PIN	53 NAB_USB3.0 TYPEC	
20 THERMAL & FAN	54 NAB_CARDREADER	
21 MCP5_MEMORY	55 NAB_PWRBTN & LID	
22 MCP5-GPIO1, LPC, BIOS ROM	56 PICKBUTTON BOARD	
23 MCP5-GPIO2	57 COVER	
24 MCP5-MISC, HDA, JTAG, SDIO	58 PVCORE_DGPU (RT3662)	
25 MCP5-PCIE, USB3, USB2	59 PVCORE_DGPU (RT8816)	
26 MCP5-CLK, RTC, CFG	60 P1V5S_DGPU (G5335Q)	
27 MCP5-DDI, EDP, CSI2, EMMC	61 P0V9S_DGPU (RT8097A)	
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SELETOR

VER.04_20171113

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TITLE MODEL, DIAGNOSTIC, FUNCTION

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 5 of 21			

CHANGE by XXX	DATE 21-OCT-2002
PCB P/N 60xxxxxxx	PCB VER XXX

Eletro-XTechnical

D

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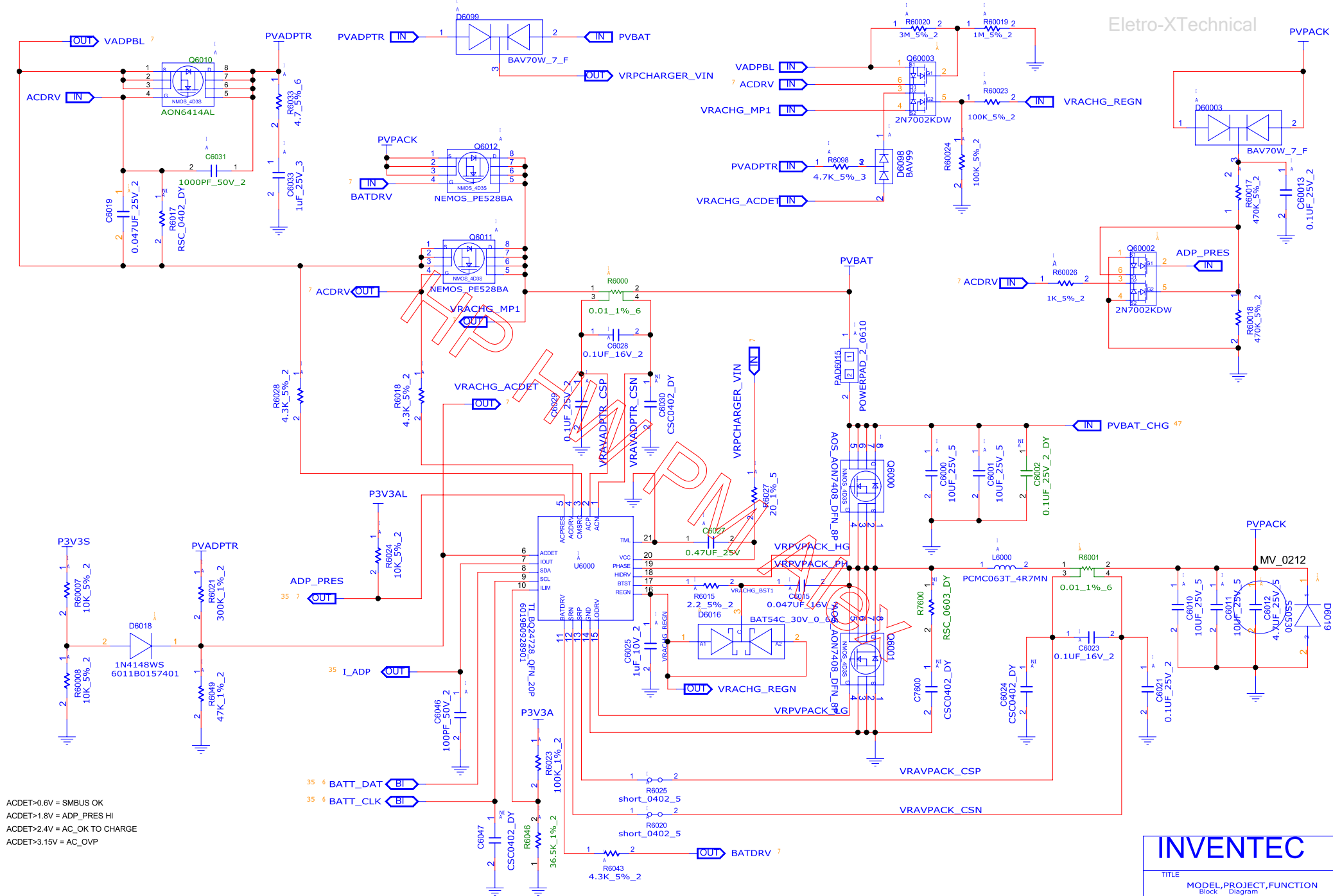
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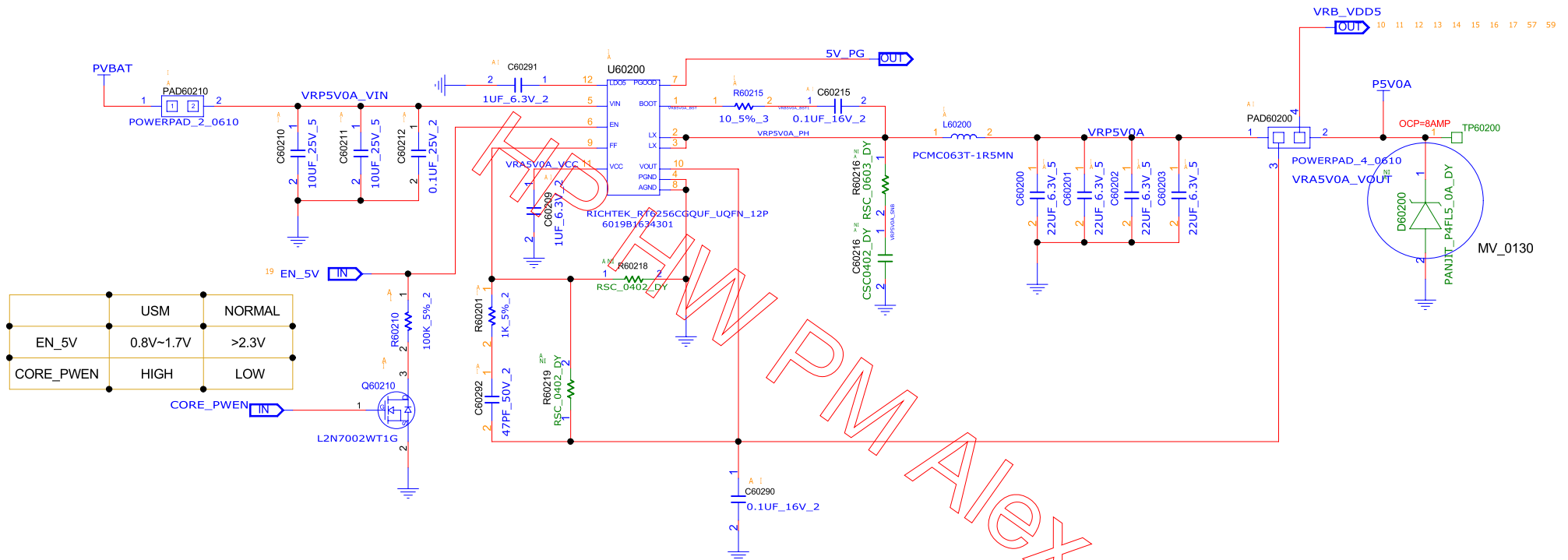


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TITLE			
MODEL, PROJECT, FUNCTION			
SIZE	CODE	DOC NUMBER	
A3	CS	1310xxxxx-0-0	
SHEET		7	of 71
REV		X01	

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX





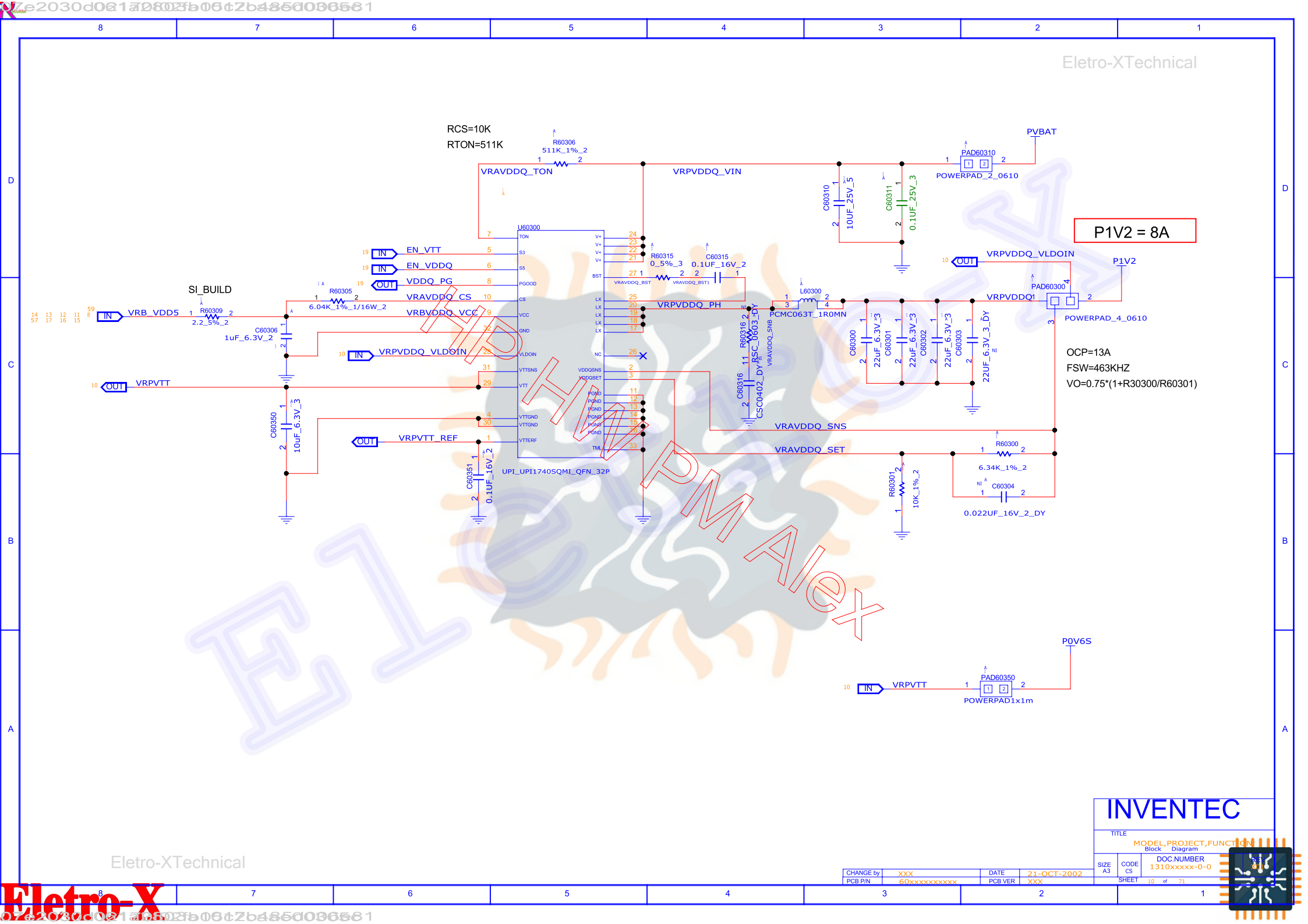
TITLE	MODEL PROJECT FUNCTION
1. Project Overview	1. Project Overview
2. Project Objectives	2. Project Objectives
3. Project Scope	3. Project Scope
4. Project Organization	4. Project Organization
5. Project Schedule	5. Project Schedule
6. Project Budget	6. Project Budget
7. Project Risk Management	7. Project Risk Management
8. Project Communication	8. Project Communication
9. Project Monitoring and Control	9. Project Monitoring and Control
10. Project Closure	10. Project Closure

DATE	CORRE	DOC. NUMBER	F
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SIZE A3	CODE CS	1310xxxxx-0-0	X
SHEET		0 of 31	

1

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



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P1V2 = 8A

OCP=13A
FSW=463KHZ
VO=0.75*(1+R30300/R60301)

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TITLE
MODEL,PROJECT,FUNCTION

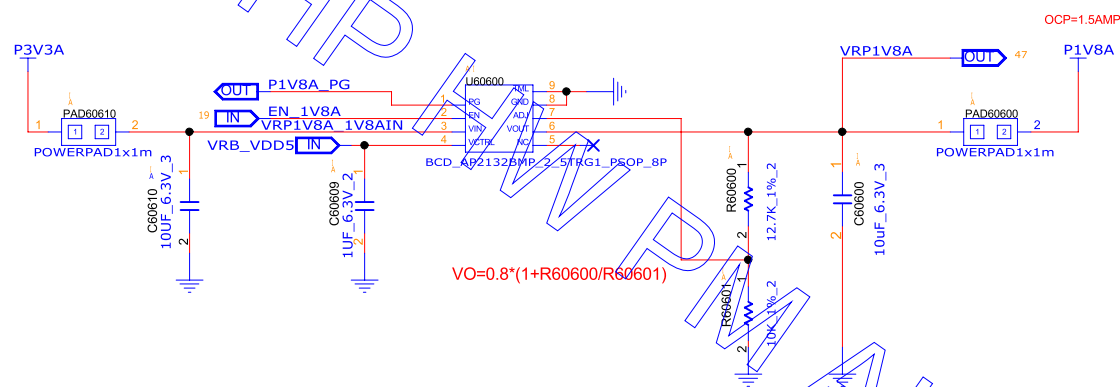
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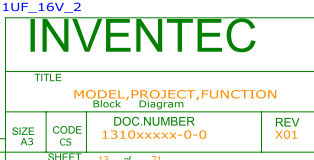
SHEET 10 of 71

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxx PCB VER XXX

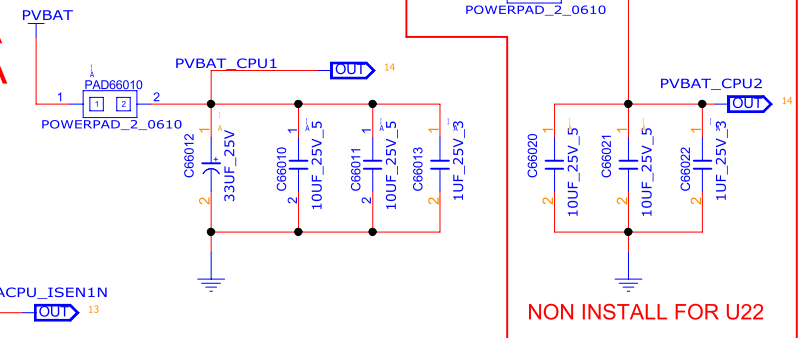
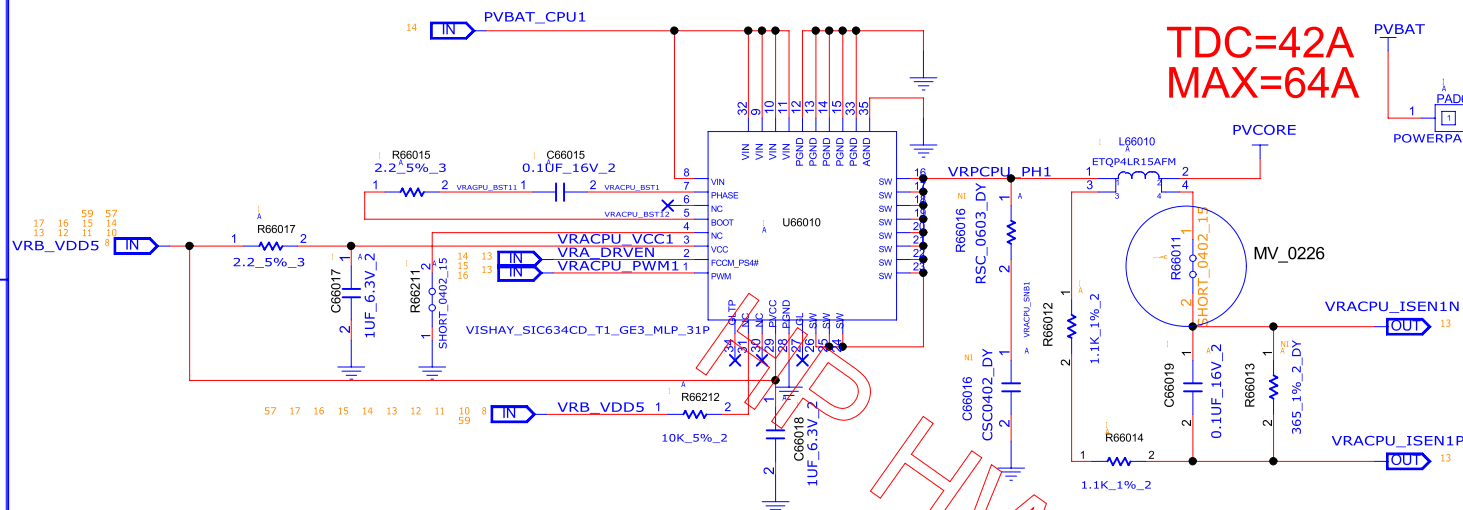
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Eletro-X

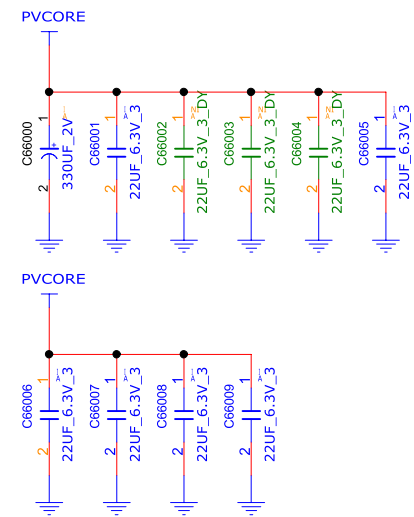
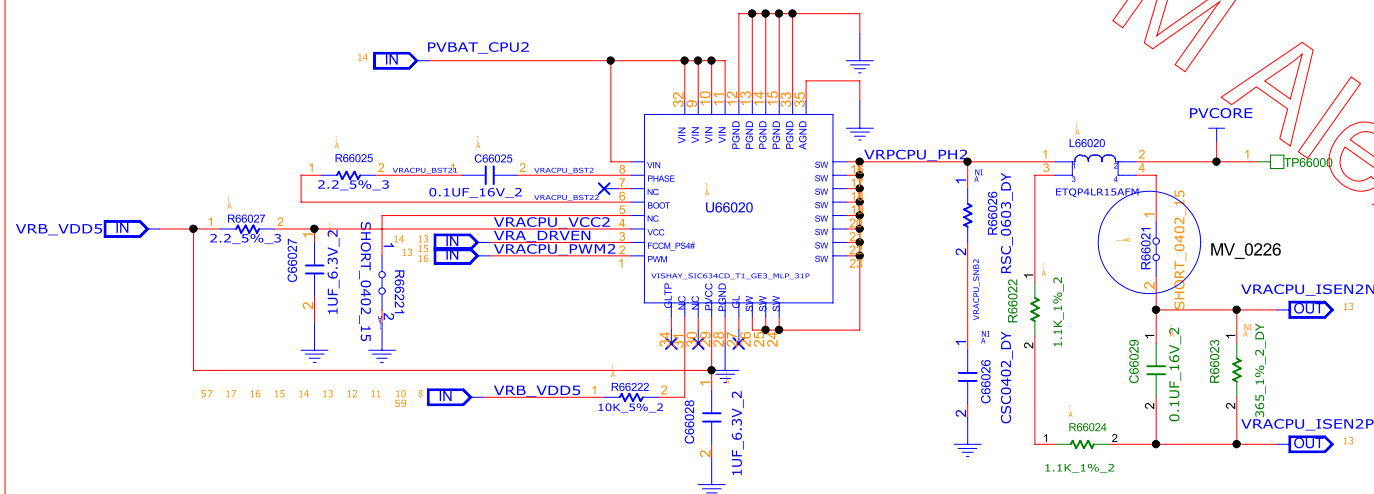




NOTE:ONE PHASE FOR U22



NOTE:NOT INSTALL FOR U22



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TITLE			
MODEL,PROJECT,FUNCTION			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 14 of 71			

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX

Eletro-XTechnical

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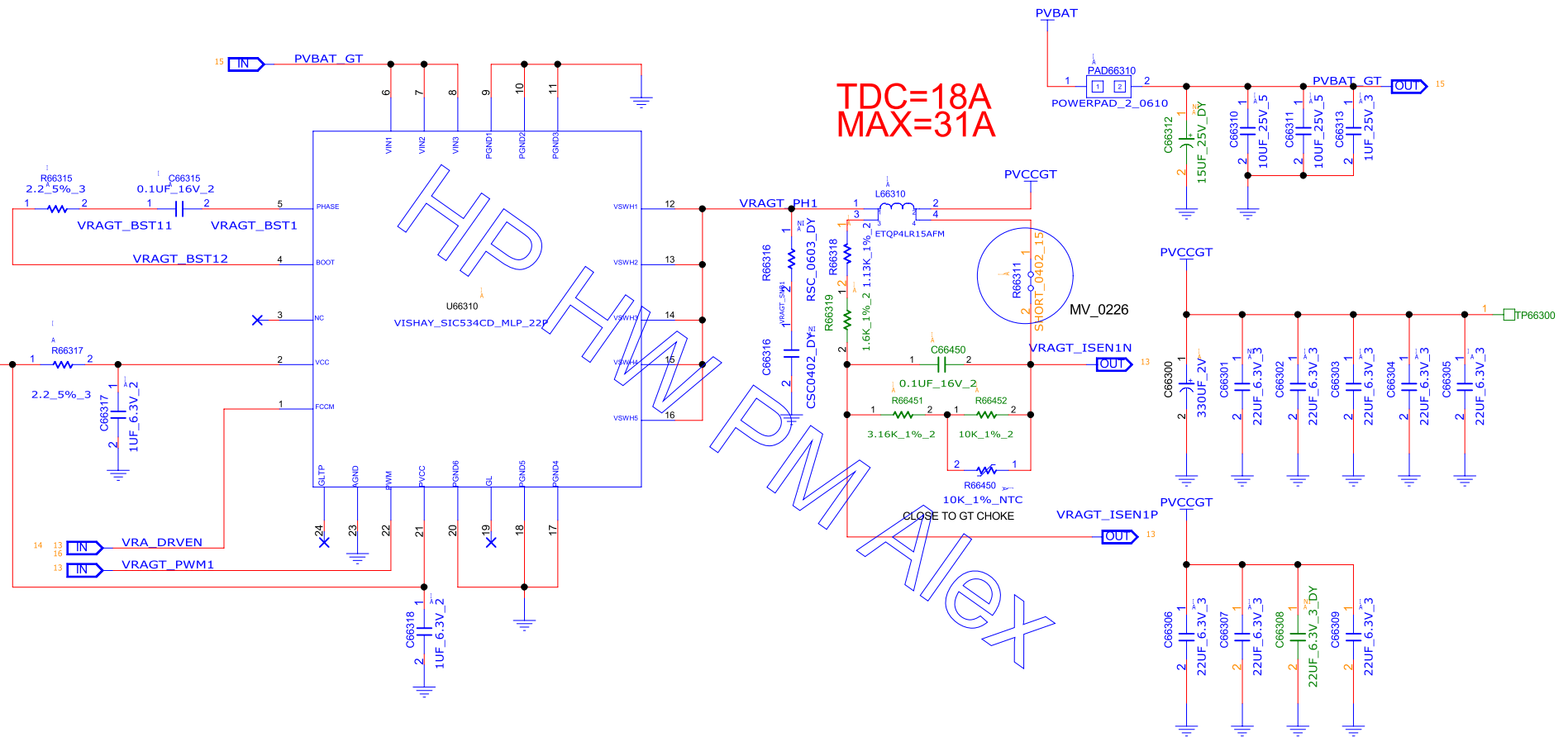
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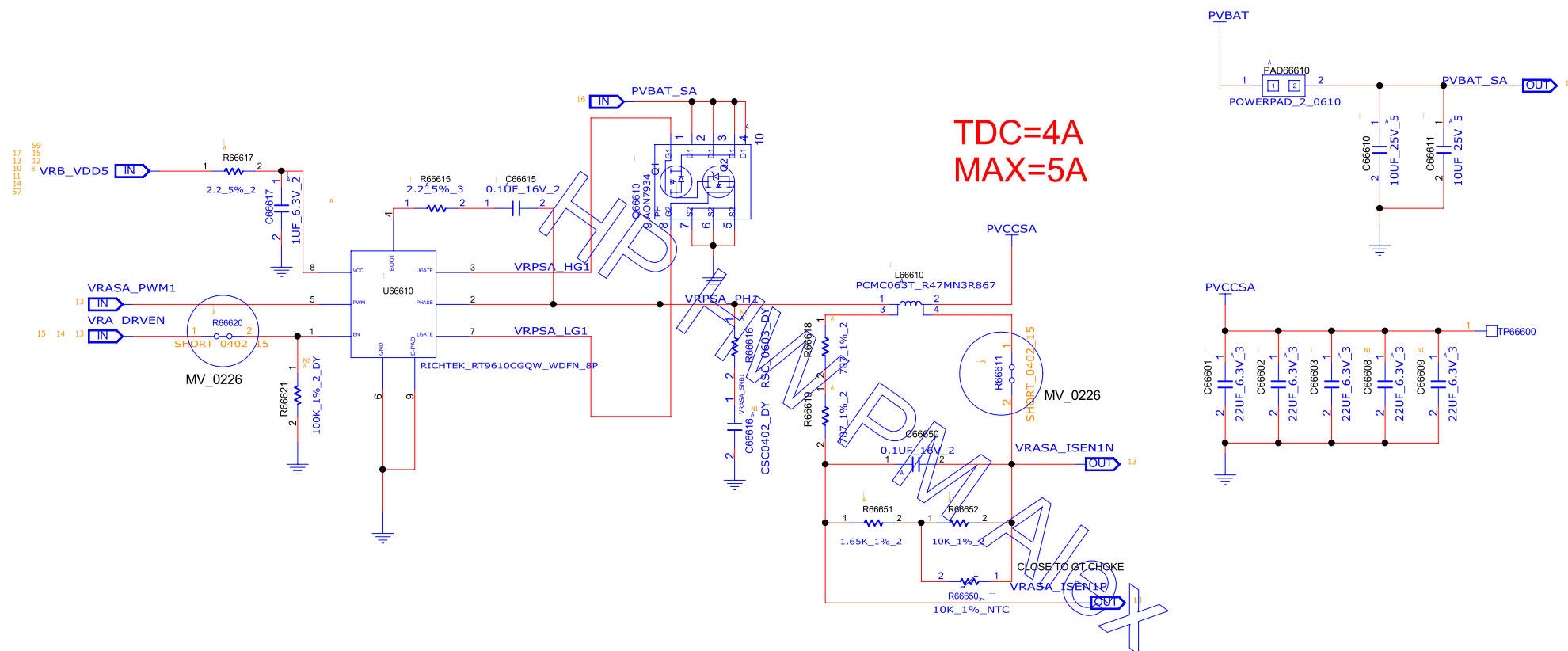
A

A



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TITLE
MODEL, PROJECT, FUNCTION
Block DiagramSIZE
A3CODE
CSSHEET
15 of 71DOC NUMBER
1310xxxxx-0-0REV
X01CHANGE by
PCB P/N
XXX
60xxxxxxxxxxDATE
PCB VER
21-OCT-2002
XXX



TDC=4A
MAX=5A

CLOSE TO GT CHOKI

~~/RASA_ISENIP)~~

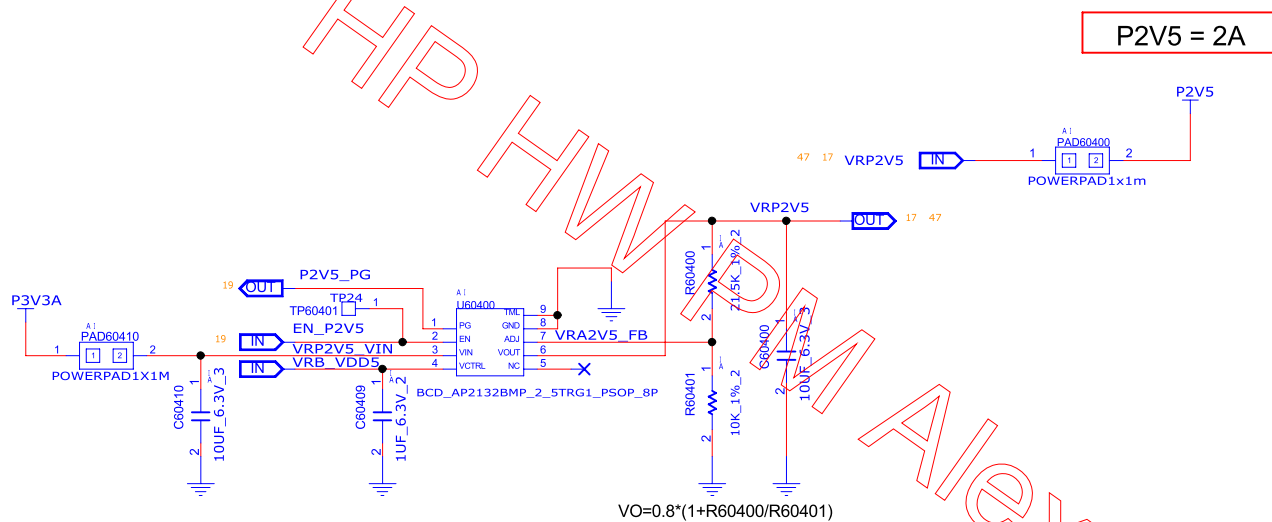
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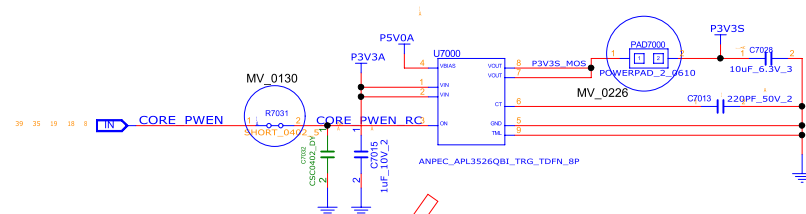
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Block Diagram	

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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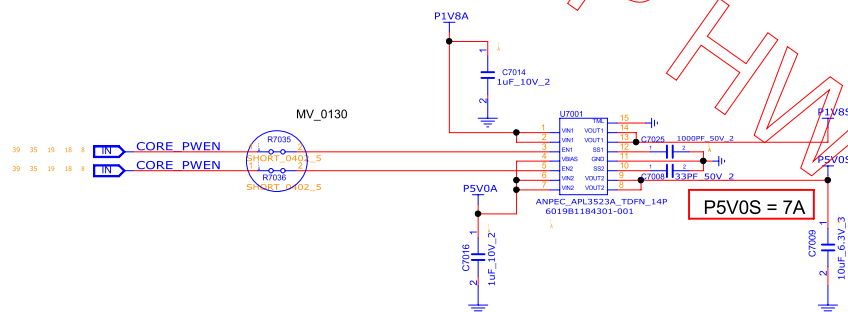
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	16	of	71		



P3V3S = 4.34A



P5V0S = 7A



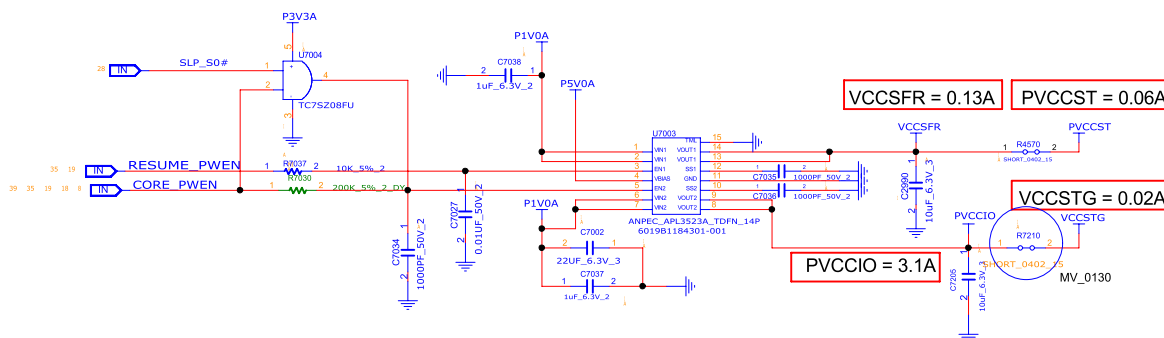
MAIN PART	MANUFACTURER	MPN	REMARKS
6019B1184301	ANPEC	APL3523AQBI-TRG	MAIN SOURCE
6019B1562901	GMT	G2898KD1U	2ND SOURCE
6019B1574101	TI	TPS22976DPUR	3RD SOURCE

VCCSFR = 0.13A

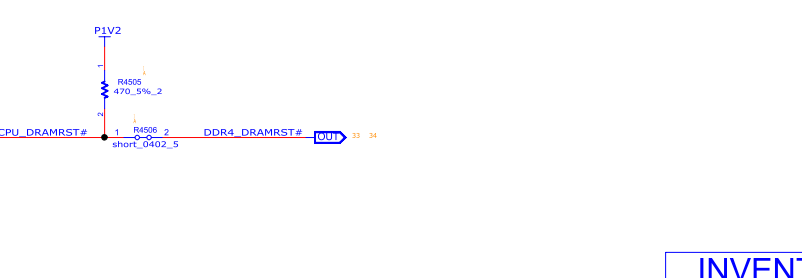
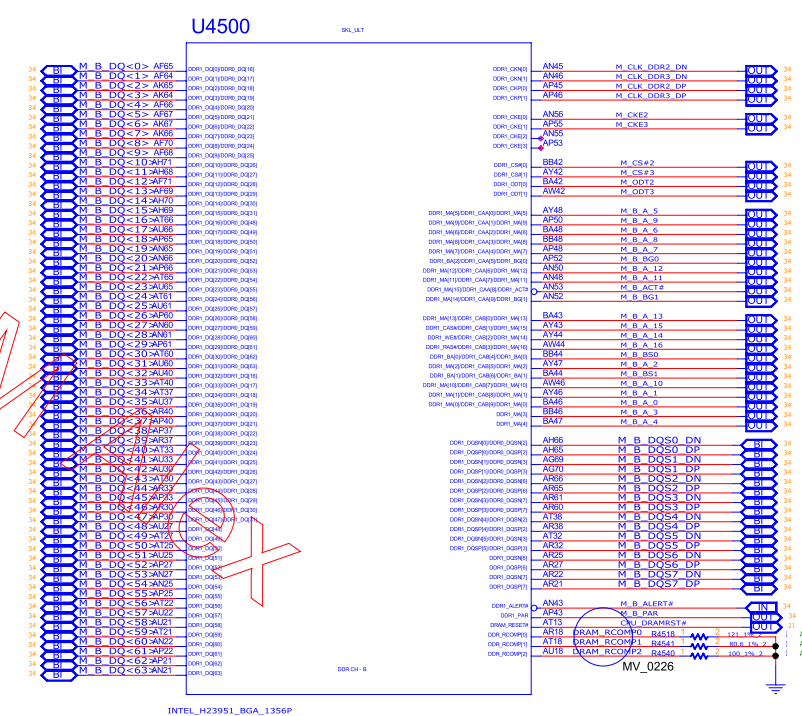
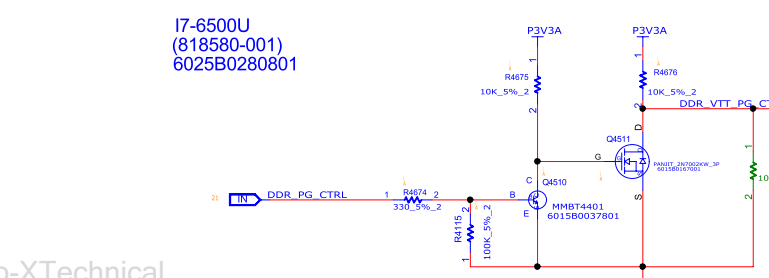
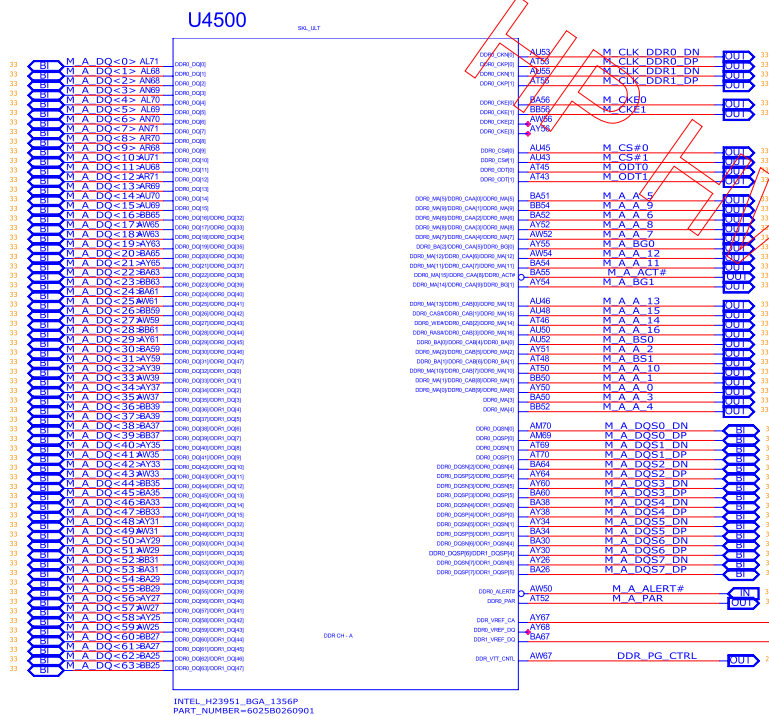
PVCCST = 0.06A

VCCSTG = 0.02A

PVCCIO = 3.1A



MAIN PART	MANUFACTURER	MPN	REMARKS
6019B1184301	ANPEC	APL3523AQBI-TRG	MAIN SOURCE
6019B1562901	GMT	G2898KD1U	2ND SOURCE
6019B1574101	TI	TPS22976DPUR	3RD SOURCE



INVENTEC

MODEL/PROJECT/FUNCTION
DDR3_SO-DIMM0

SIZE C CODE CS XXXNUMBER REV X01

CHANGE IN PCB PIN XXX DATE PCB VER 2.0

SHEET 1

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ALL UNUSED GPIOs (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION

All GPIOs have weak internal pull-up/down resistors which are off by default.
The Internal PU/PD can be programmed (PU/PD/None) by BIOS after reset.

GPIO GROUP SUMMARY		
GPIO GROUP	POWER PINS	VOLTAGE
PRIMARY WELL GROUP A (GPP_A)	VCCPGPPA	1.8V OR 3.3V
PRIMARY WELL GROUP B (GPP_B)	VCCPGPPB	1.8V OR 3.3V
PRIMARY WELL GROUP C (GPP_C)	VCCPGPPC	1.8V OR 3.3V
PRIMARY WELL GROUP D (GPP_D)	VCCPGPPD	1.8V OR 3.3V
PRIMARY WELL GROUP E (GPP_E)	VCCPGPPE	1.8V OR 3.3V
PRIMARY WELL GROUP F (GPP_F)	VCCPGPPF	1.8V
PRIMARY WELL GROUP G (GPP_G)	VCCPGPPG	1.8V OR 3.3V
DEEP SLEEP WELL GROUP (GPD)	VCCPDSW_3P3	3.3V

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P3V3A

TLS CONFIDENTIALITY GPP_C2
(INTERNAL PULL DOWN 20K)

OUT TLS

THIS SIGNAL HAS A WEAK INTERNAL PULL-DOWN.
0 = DISABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) CIPHER SUITE (NO CONFIDENTIALITY).
1 = ENABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) CIPHER SUITE (WITH CONFIDENTIALITY). MUST BE PULLED UP TO SUPPORT INTEL AMT WITH TLS AND INTEL SBA (SMALL BUSINESS ADVANTAGE) WITH TLS.

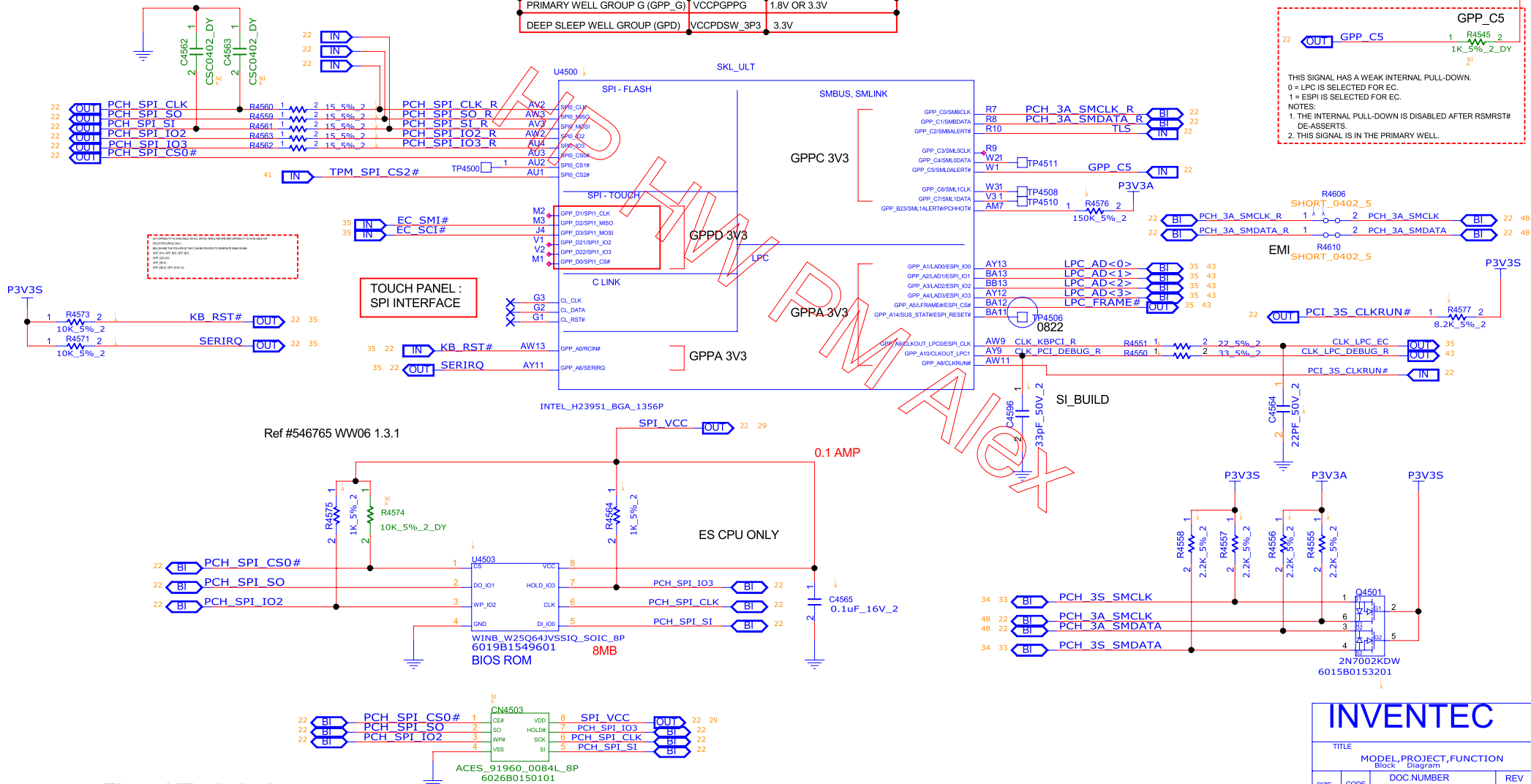
NOTES:
1. THE INTERNAL PULL-DOWN IS DISABLED AFTER RSMRST# DE-ASSERTS.
2. THIS SIGNAL IS IN THE PRIMARY WELL.

GPP_C5

OUT GPP_C5

THIS SIGNAL HAS A WEAK INTERNAL PULL-DOWN.
0 = LPC IS SELECTED FOR EC.
1 = ESPI IS SELECTED FOR EC.

NOTES:
1. THE INTERNAL PULL-DOWN IS DISABLED AFTER RSMRST# DE-ASSERTS.
2. THIS SIGNAL IS IN THE PRIMARY WELL.





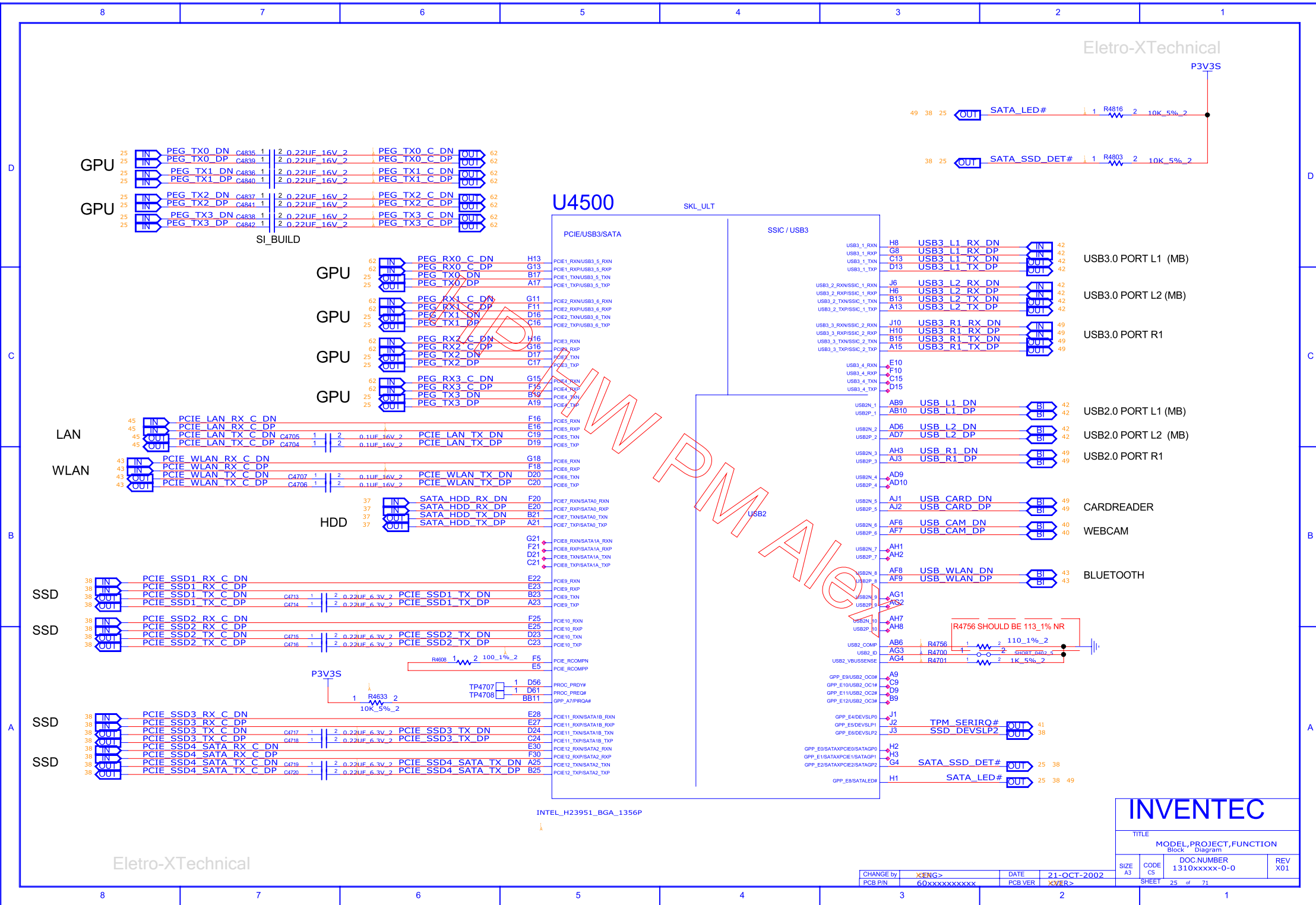
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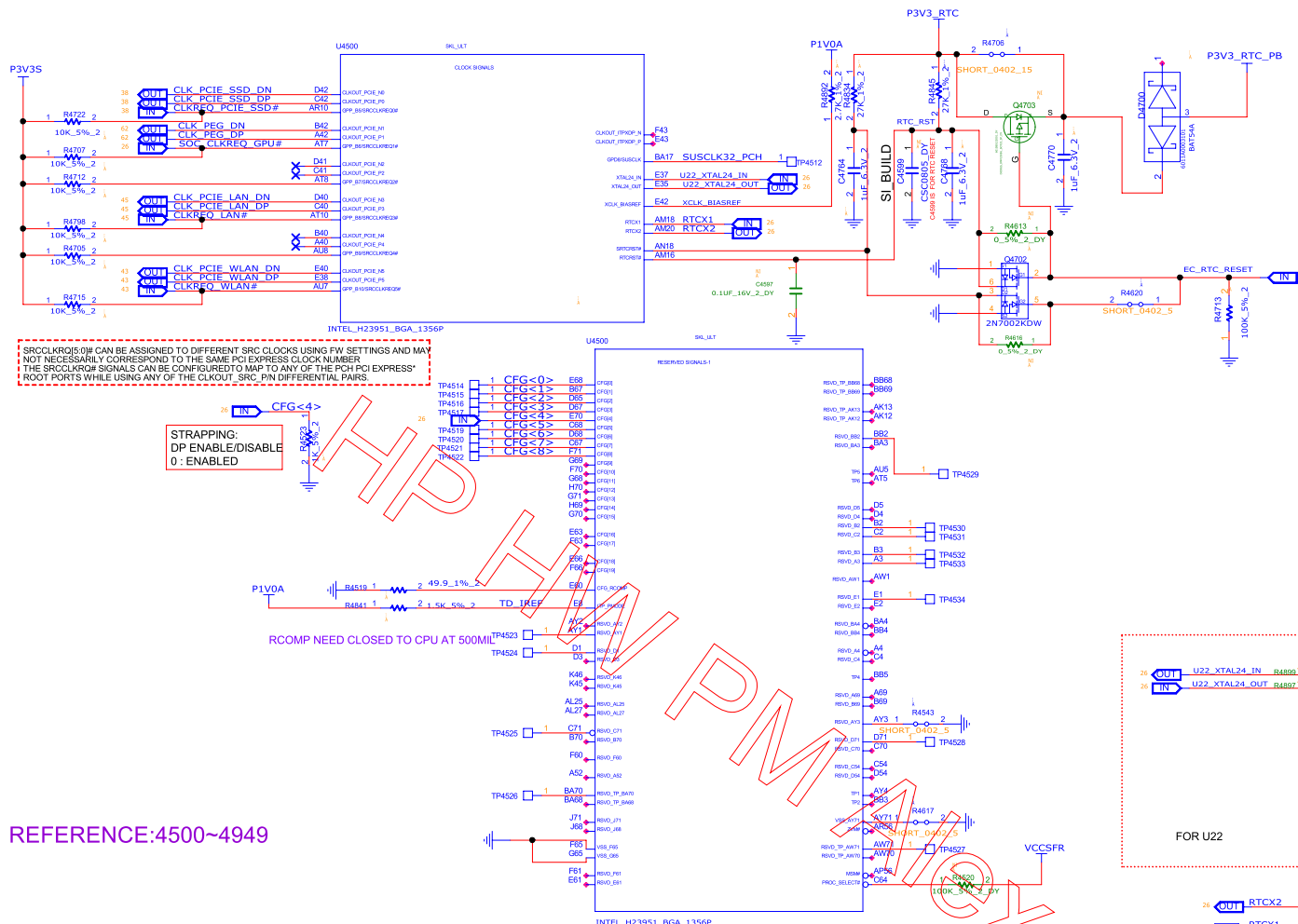
PLATFORM		RAM_ID0	RAM_ID1	RAM_ID2	RAM_ID3
17 KBL-U	T.B.D	0	0	0	0



TITLE	MODEL,PROJECT,FUNCTION
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SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 24 of 71			



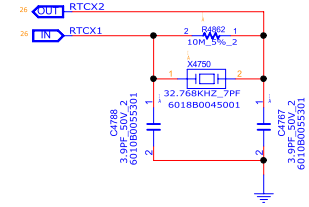
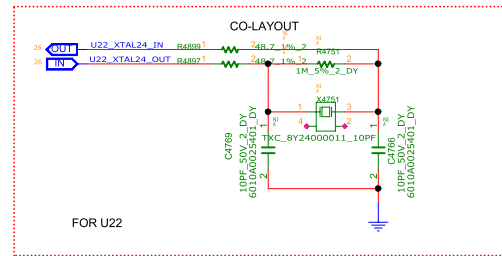
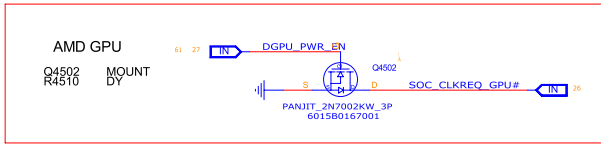


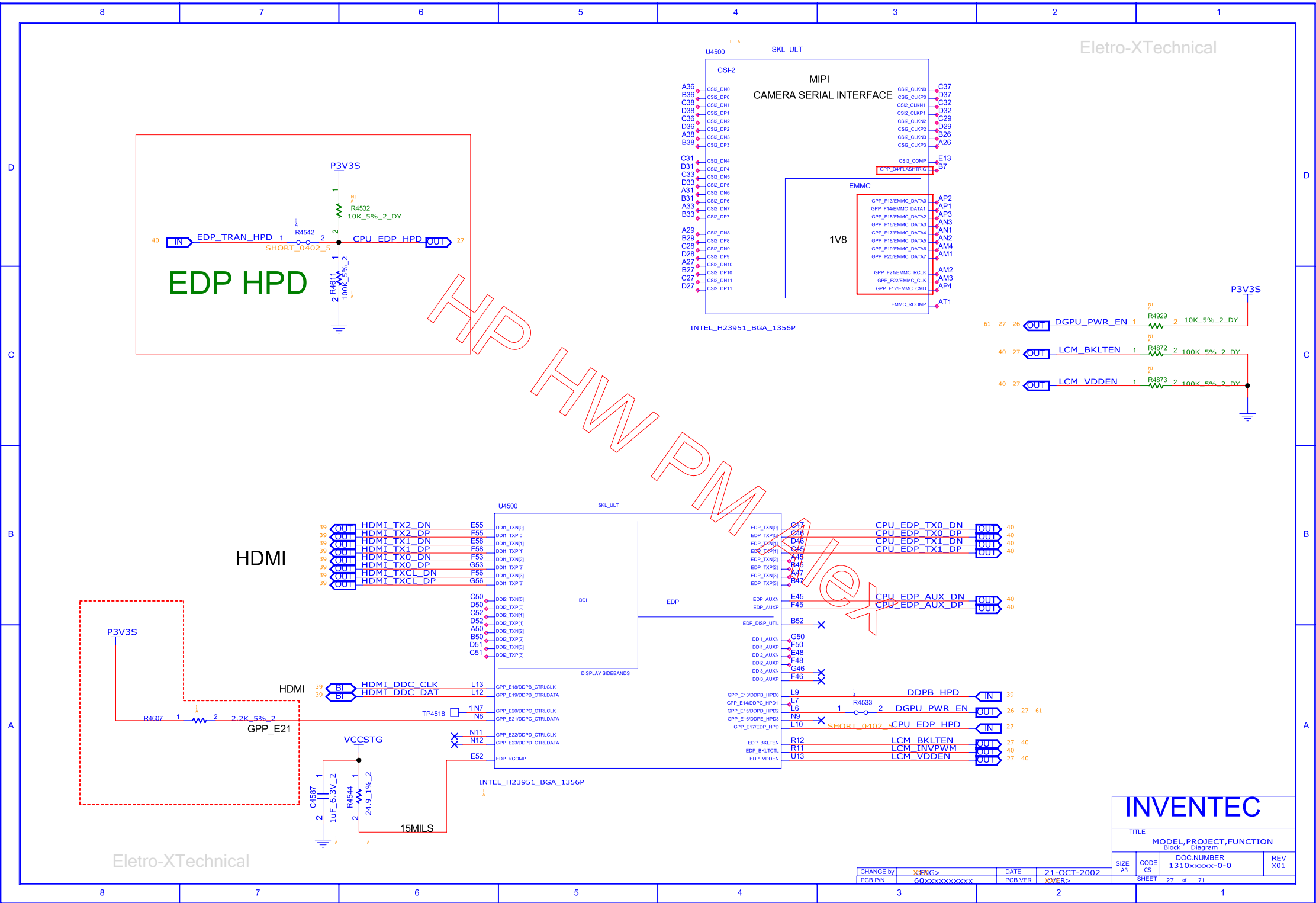
INTEL_H23951_BGA_1356P

STRAPPING:
DP ENABLE/DISABLE
0: ENABLED

RCOMP NEED A TO CPU AT 500MIL

REFERENCE:4500-4949





D

C

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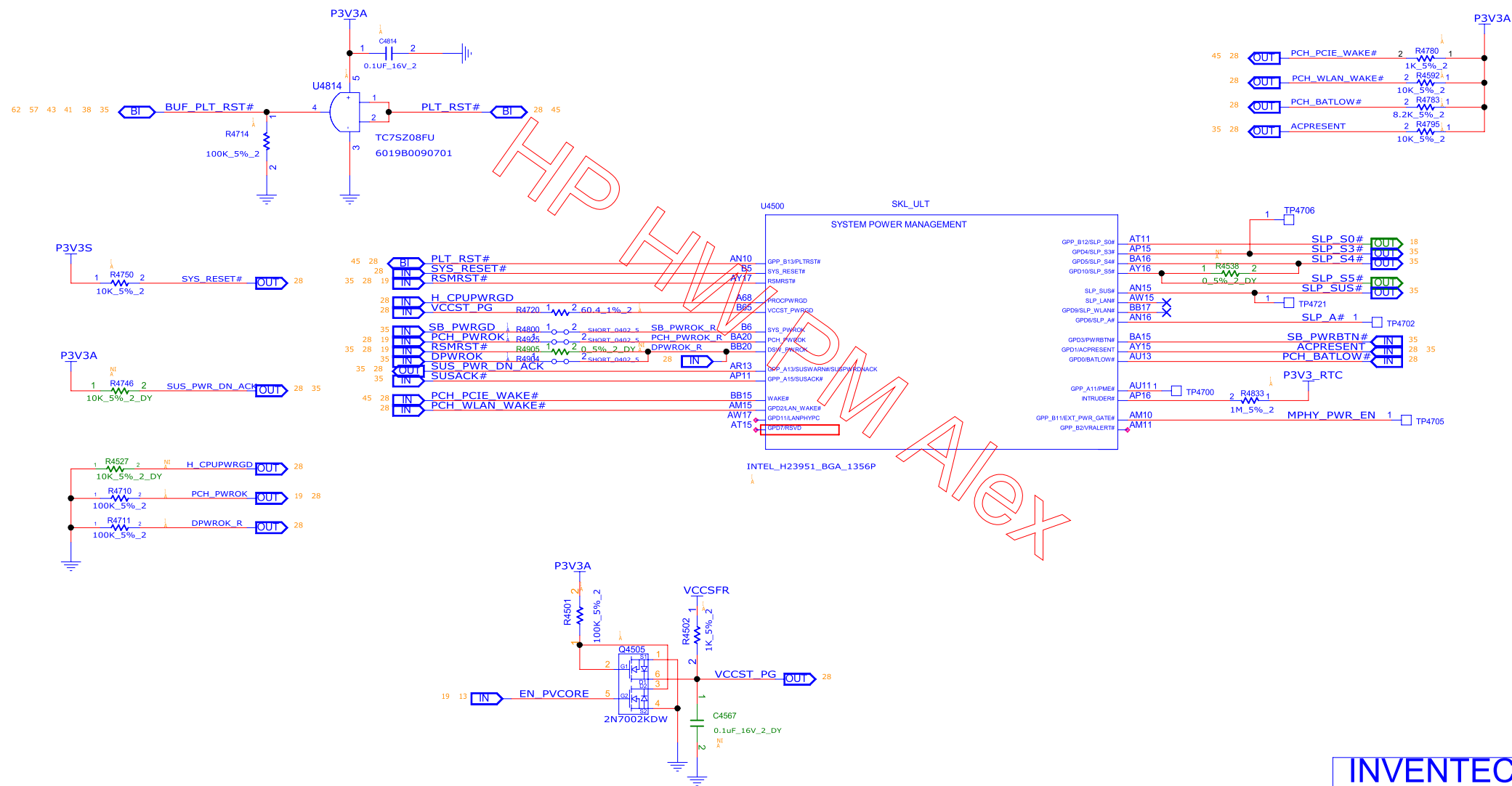
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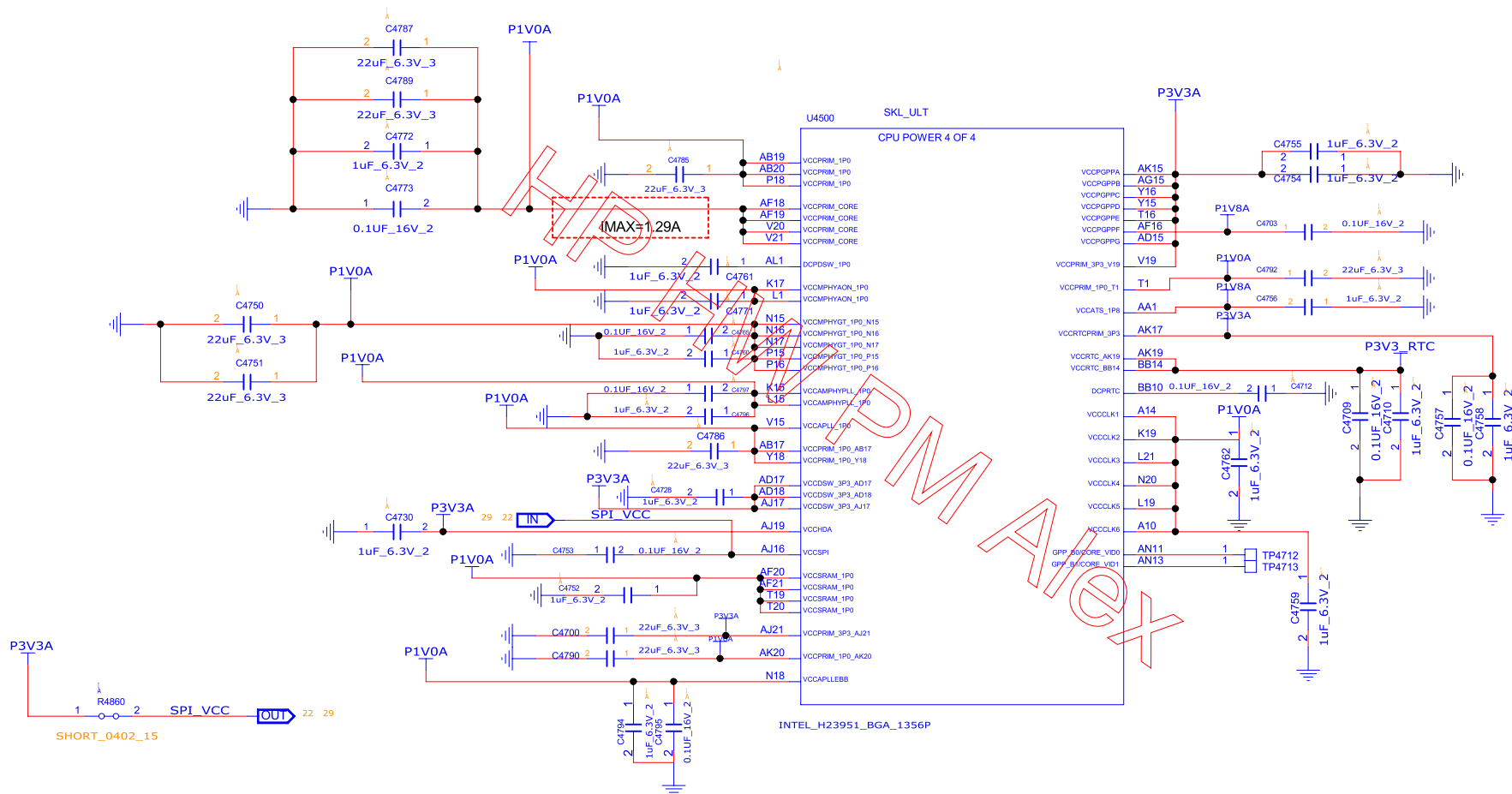
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TITLE
MODEL, PROJECT, FUNCTIONDOC NUMBER
1310xxxxx-0-0REV
X01CHANGE by
PCB P/N
XENG>
60xxxxxxxxxxxDATE
PCB VER
21-OCT-2002
XVER>SHEET
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REFERENCE 4700~4949(PCH)

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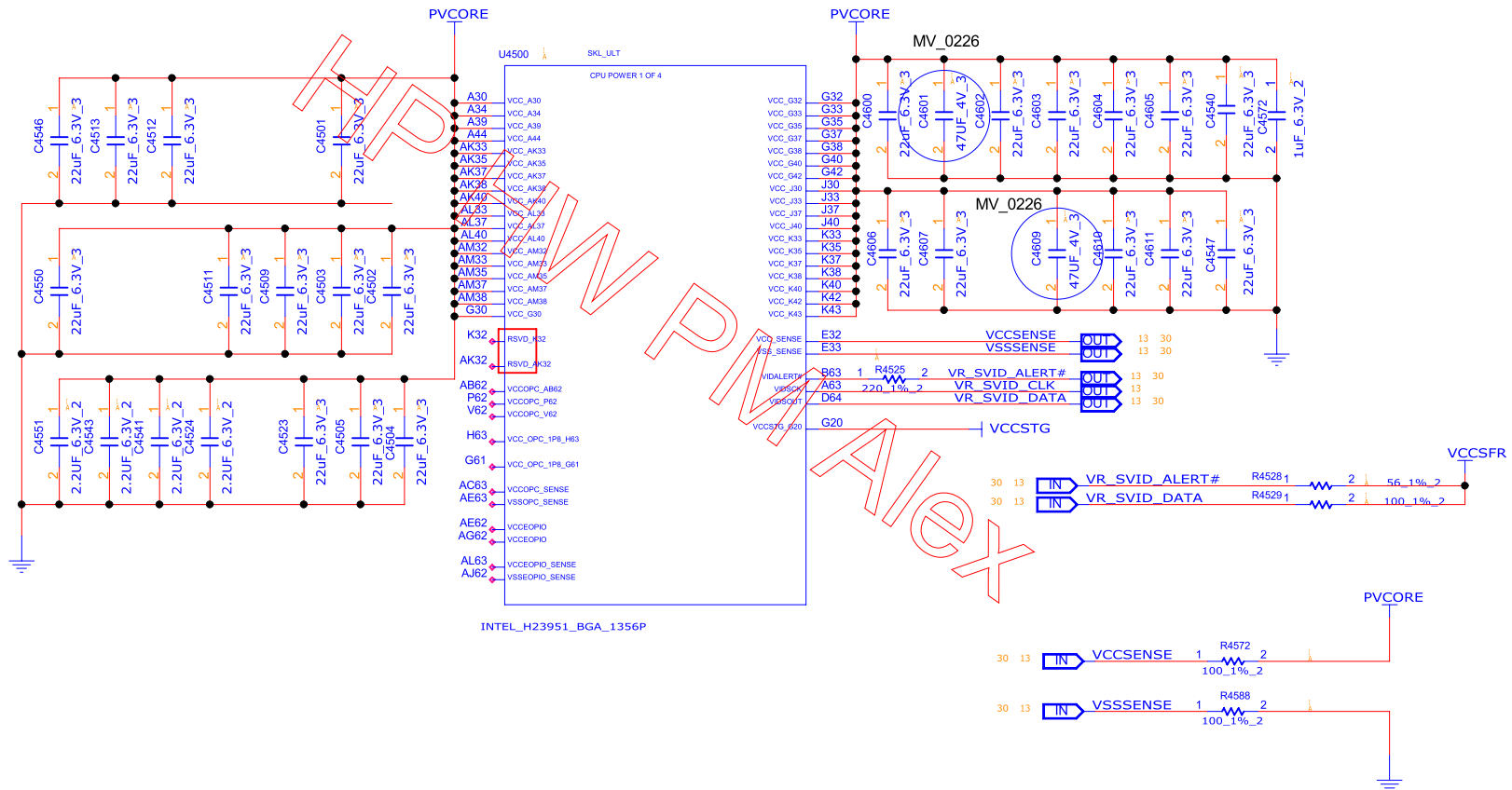
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MODEL, PROJECT, FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

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CHANGE by XXX PCB P/N 60NSxxxxxxx DATE PCB VER 00000000-2002

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INVENTEC

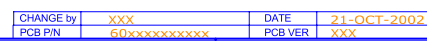
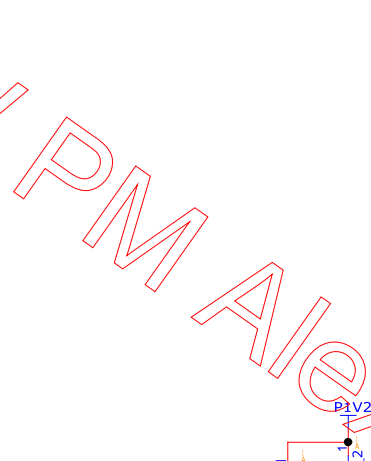
TITLE
MODEL, PROJECT, FUNCTIONDOC NUMBER
1310xxxxx-0-0REV
X01

SHEET 30 of 71

CHANGE by: XENG>
PCB P/N: 60xxxxxxxxxxxDATE: 21-OCT-2002
PCB VER: XVER>



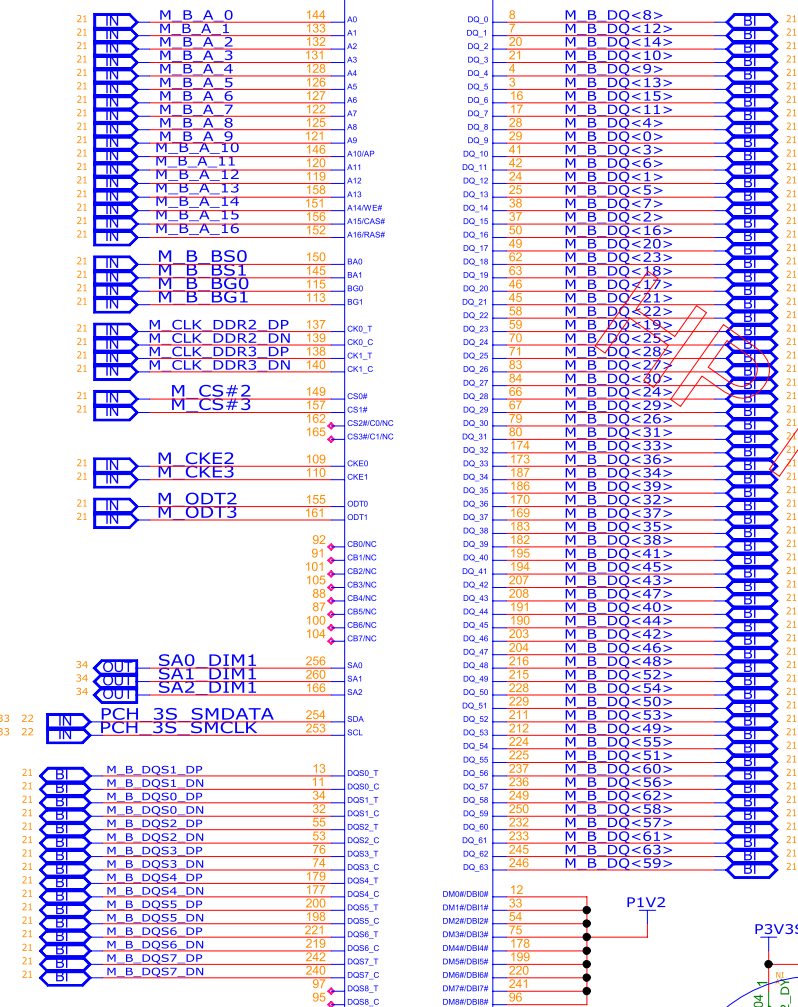
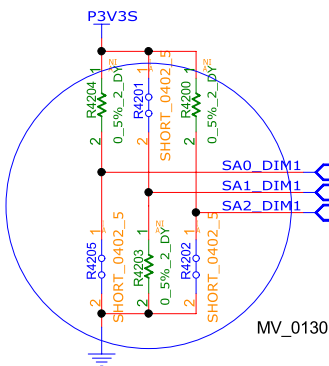
CN4200



REFERENCE 4100~4299(DDR)

CHB
H=4

CN4100

ARGOSY_D4AR0_26010_1P40_260P
6026B0328101-004

MV_0130

SPD ADDRESS FOR CHANNEL-1

WRITE ADDRESS:0XA4

RED ADDRESS :0XA3

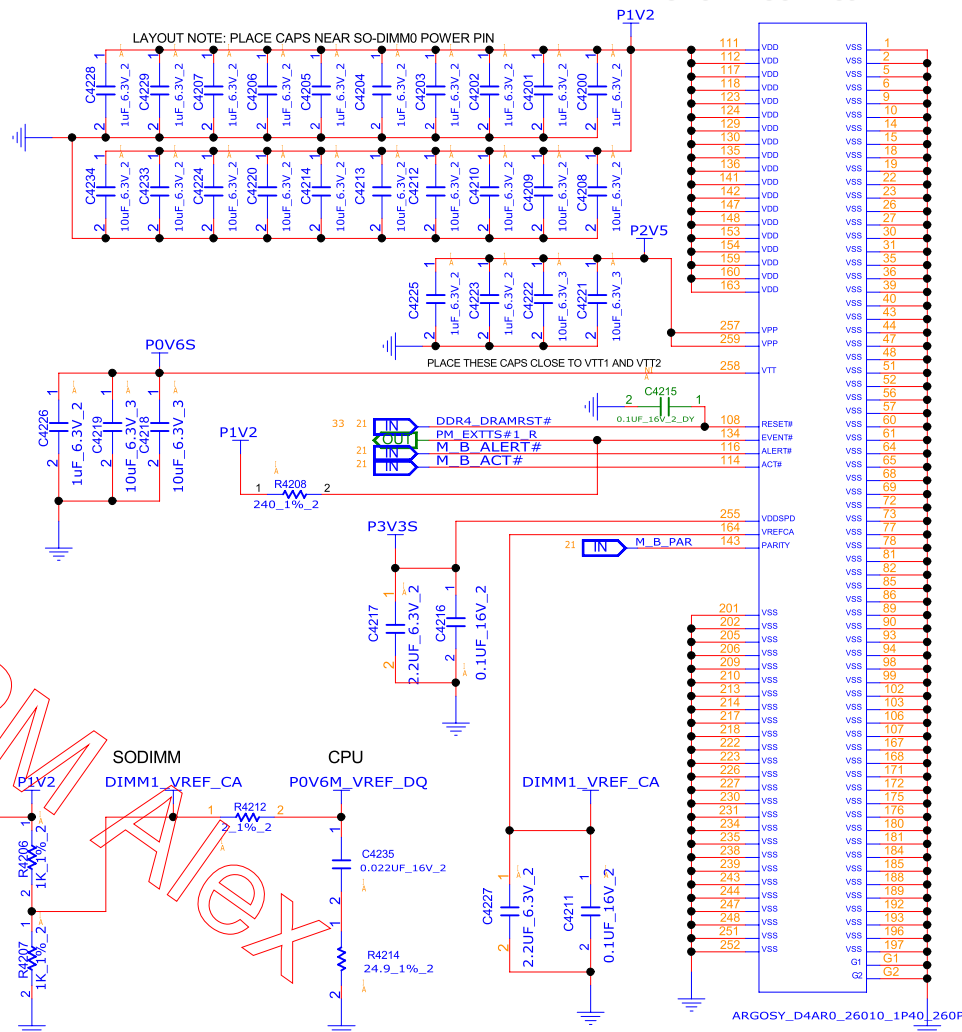
SA0=0,SA1=1,SA2=0

DDR4 FOR OPERATING SPEED:1867 MT/S

STRETCH GOAL IS 2133 MT/S

EVENT_N: INDICATES THERMAL EVENT ON DIMM.

EVENT_N:ON ECC DIMM:KEEP A PULL UP IF NO PIN IN PCH

CN4100
Eletro-XTechnical

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

DOC NUMBER

1310xxxxx-0-0

REV

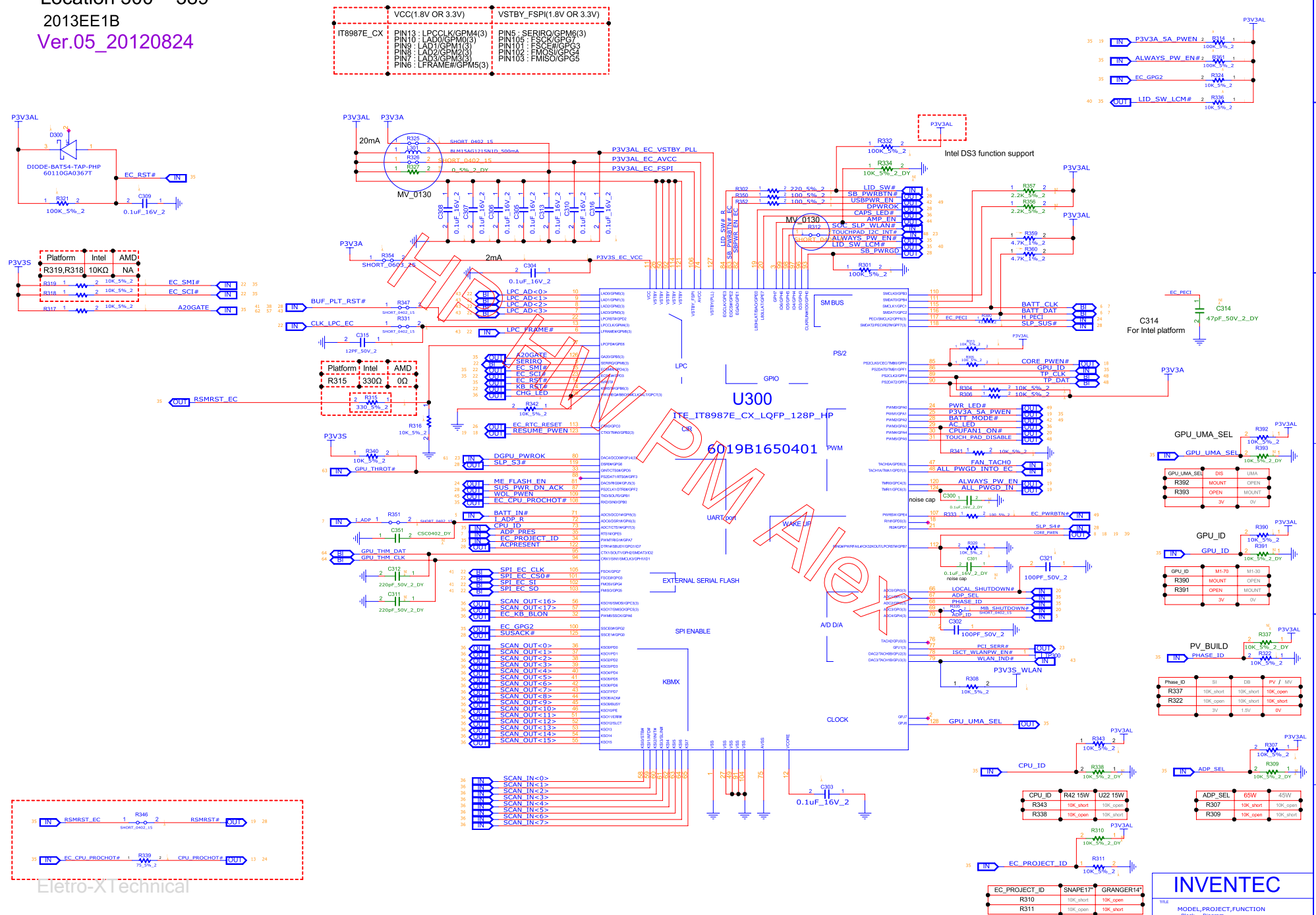
X01

SHEET 34 of 71

CHANGE by XXX
PCB P/N 60xxxxxxxDATE 21-OCT-2002
PCB VER XXX

Location 300 ~ 389
2013EE1B
Ver.05_20120824

Eletro-XTechnical



INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
-------	--------------------------

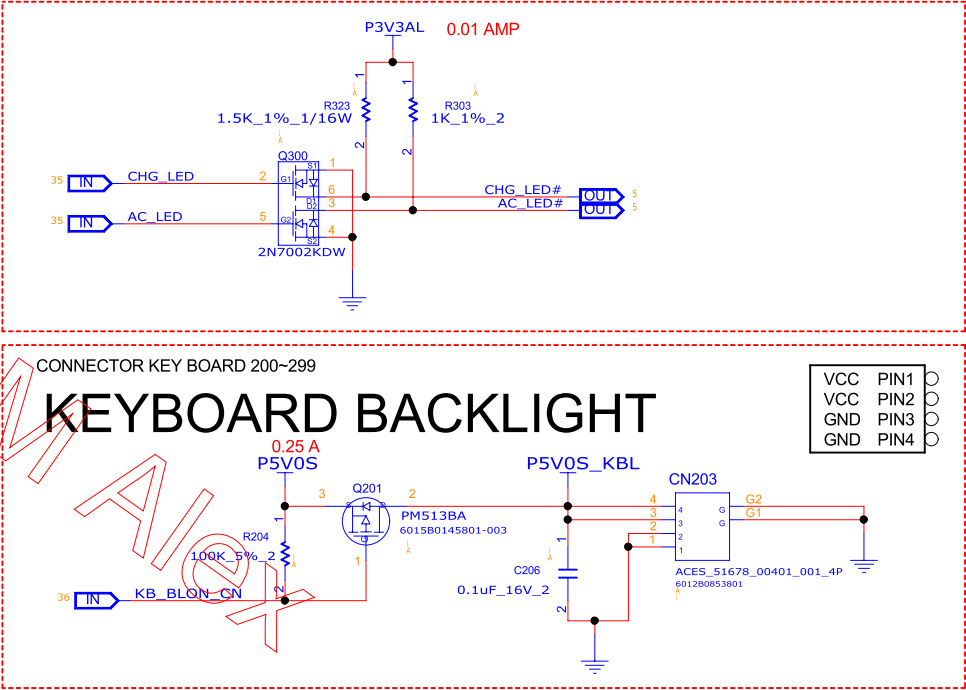
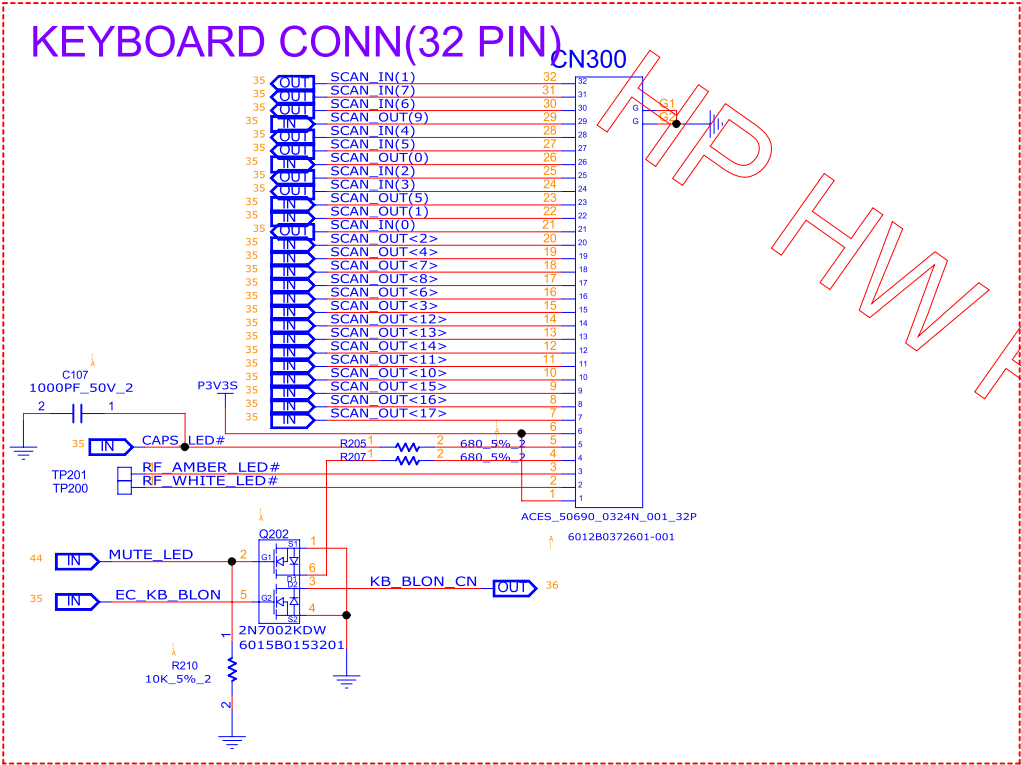
CHANGE by	xxx	DATE	21-OCT-2002
PCB PIN	60xxxxxxxxxx	PCB VER	xxx

SIZE A3	CODE CS	DOC NUMBER 1310xxxxxx-C
SHEET		35 of 71

KEYBOARD CONNECTOR

VER.07_20171110

Eletro-XTechnical



INVENTEC

TITLE MODEL PROJECT,FUNCTION

DOC NUMBER 1310xxxxx-0-0

REV X01

SHEET 36 of 71

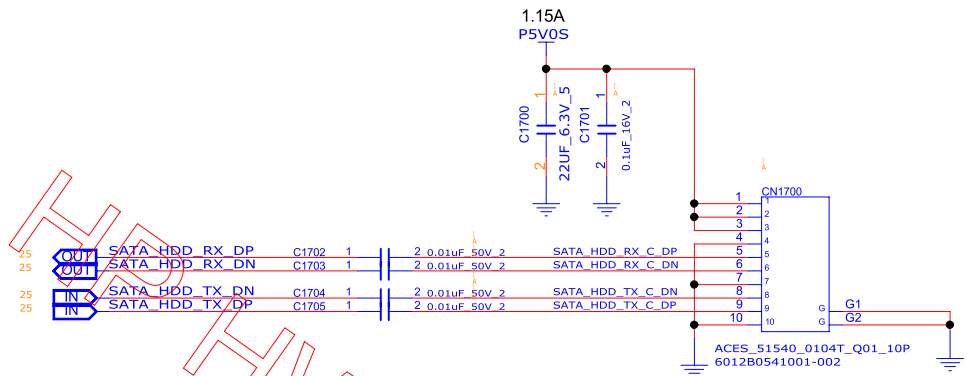
CHANGE by XENG> DATE 21-OCT-2002

PCB P/N 60xxxxxxx PCB VER XVER>

Eletro-XTechnical

SATA HDD CABLE CONN on MB

VER.01_20170918



INVENTEC

TITLE
MODEL PROJECT FUNCTION
SATA_HDD & SATA_ODD

SIZE
A3

CODE
CS

DOC NUMBER
1310xxxxx-0-0

REV
X01

SHEET
of 37 71

CHANGE by
PCB P/N

DATE
PCB VER

DATE
PCB VER

DATE
PCB VER

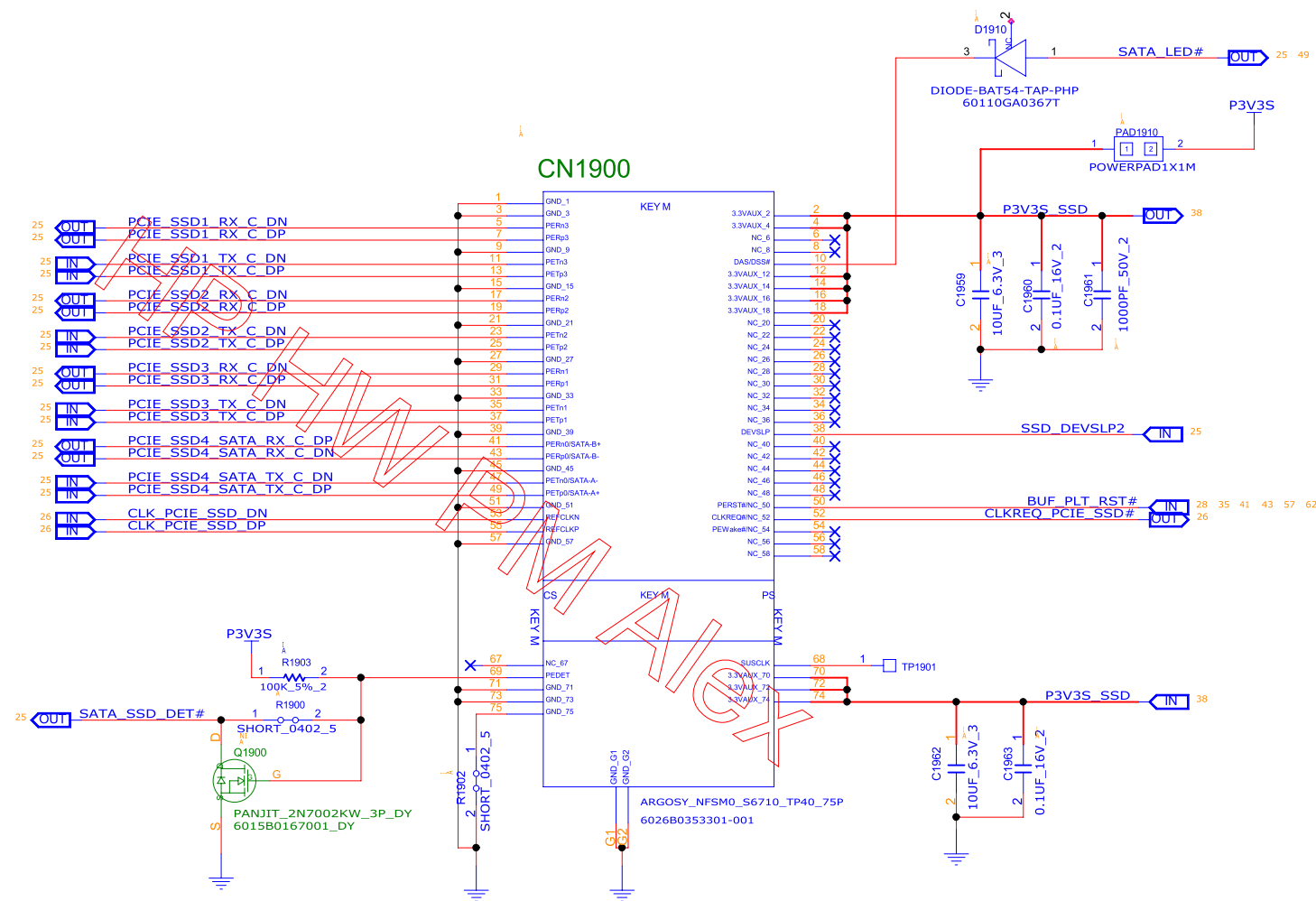
Eletro-XTechnical

M.2 SSD

REFERENCE NUMBER:1900~1949

VER.03_20171004

Eletro-XTechnical



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

SHEET of 38 71

CHANGE by XENG> DATE 21-OCT-2002
PCB P/N 60xxxxxxx PCB VER XVER>

Eletro-XTechnical

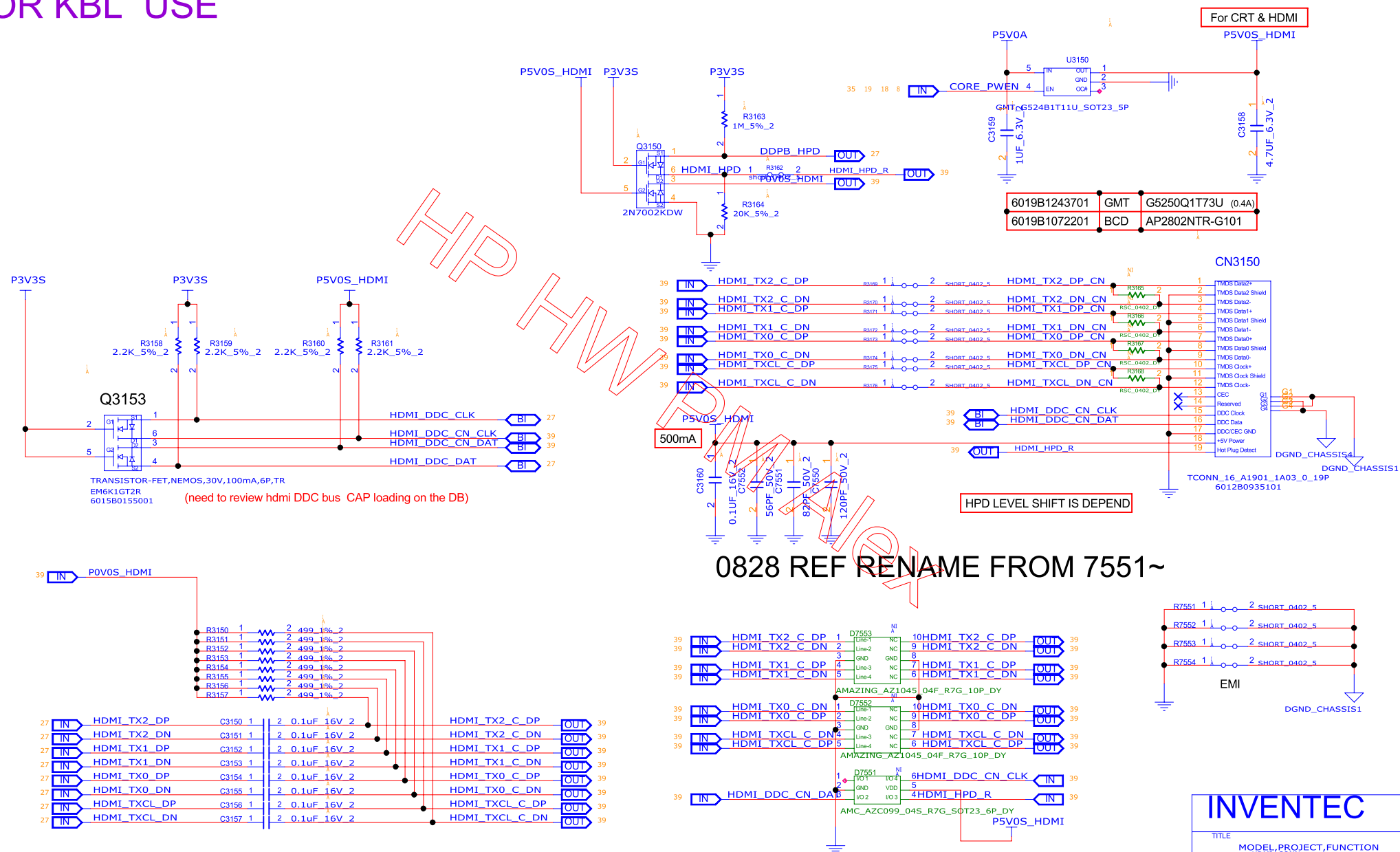
HDMI

Location 3150 ~ 3199

VER.08 20171115-2

FOR KBL USE

Eletro-XTechnical



0828 REF RENAME FROM 7551~

INVENTEC

TITLE	MODEL PROJECT FUNCTION
-------	------------------------

MODEL, PROJECT, FUNCTION			
HDMI_CONN			
	----	DOC. NUMBER	

SIZE A3	CODE CS	1310xxxxx-0-0	X
SHEET 33 of 34			

SHEET 39 of 71

VER.14 20171119

0918-2 LCM CONN MODIFY SCHEMATIC



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION LVDS			
SIZE C	CODE CS	DOC NUMBER 1310XXXXX-0-0	REV X01
SHEET		of 40	71

CHANGE by	xxx	DATE	
PCB PIN	60xxxxxxx	PCB VER 2	1-000002

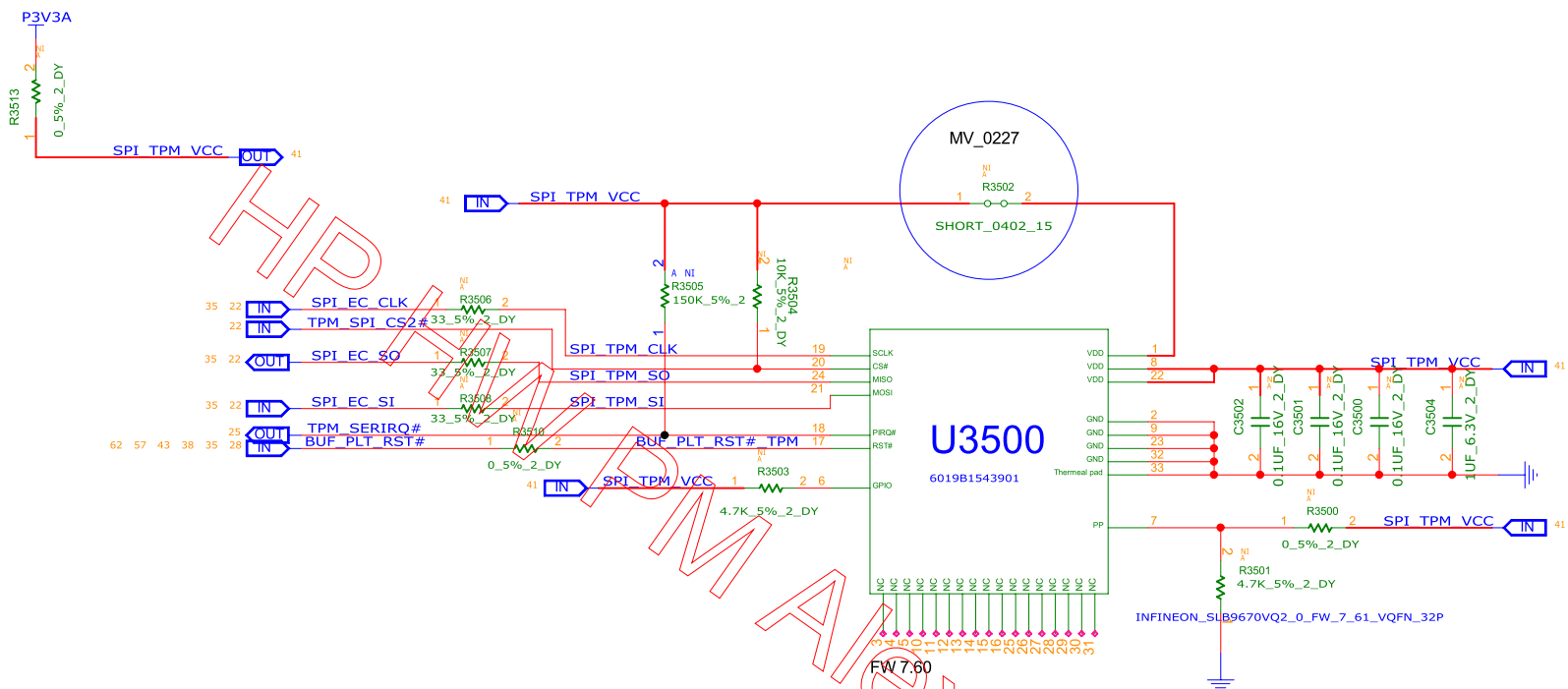
TPM2.0

REFERENCE 3500 ~ 3599

Eleto-XTechnical

FOR BIG CORE USE

VER.03_20171109

FW 7.61
6019B1543901
INFINEON SLB9670VQ2 0 FW 7 61 VQFN 32P

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION
-------	------------------------

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 41 of 71			

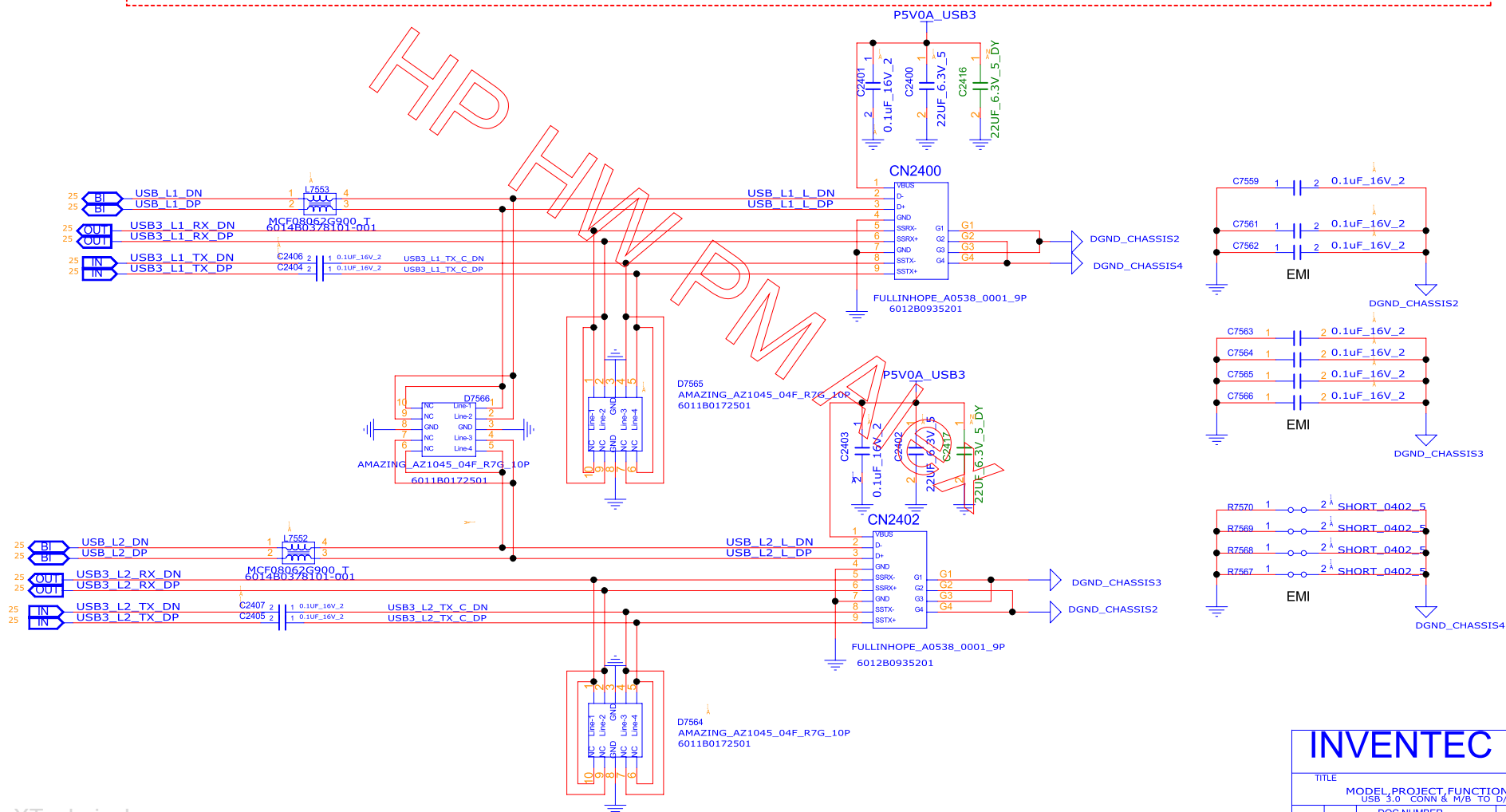
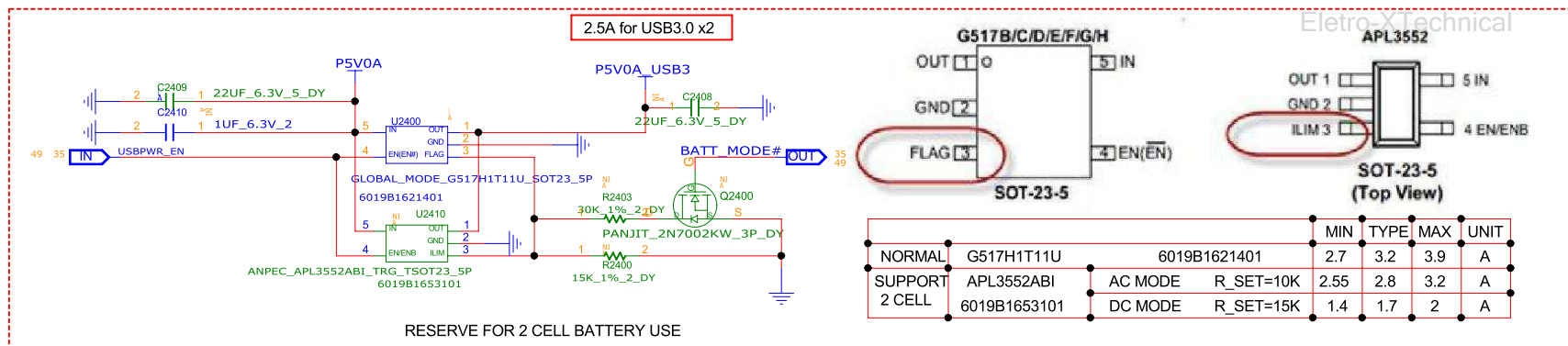
Eletro-XTechnical

CHANGE by	XJENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XVER>

USB3.0

LOCATION 2400~2499

VER.08_20171119



INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
USB 3.0 CONN & R/B TO D/B CONN			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		of 42	71

CHANGE by	XXX	DATE	
PCB P/N	6019B1653101	PCB VER	VER.08_20171119

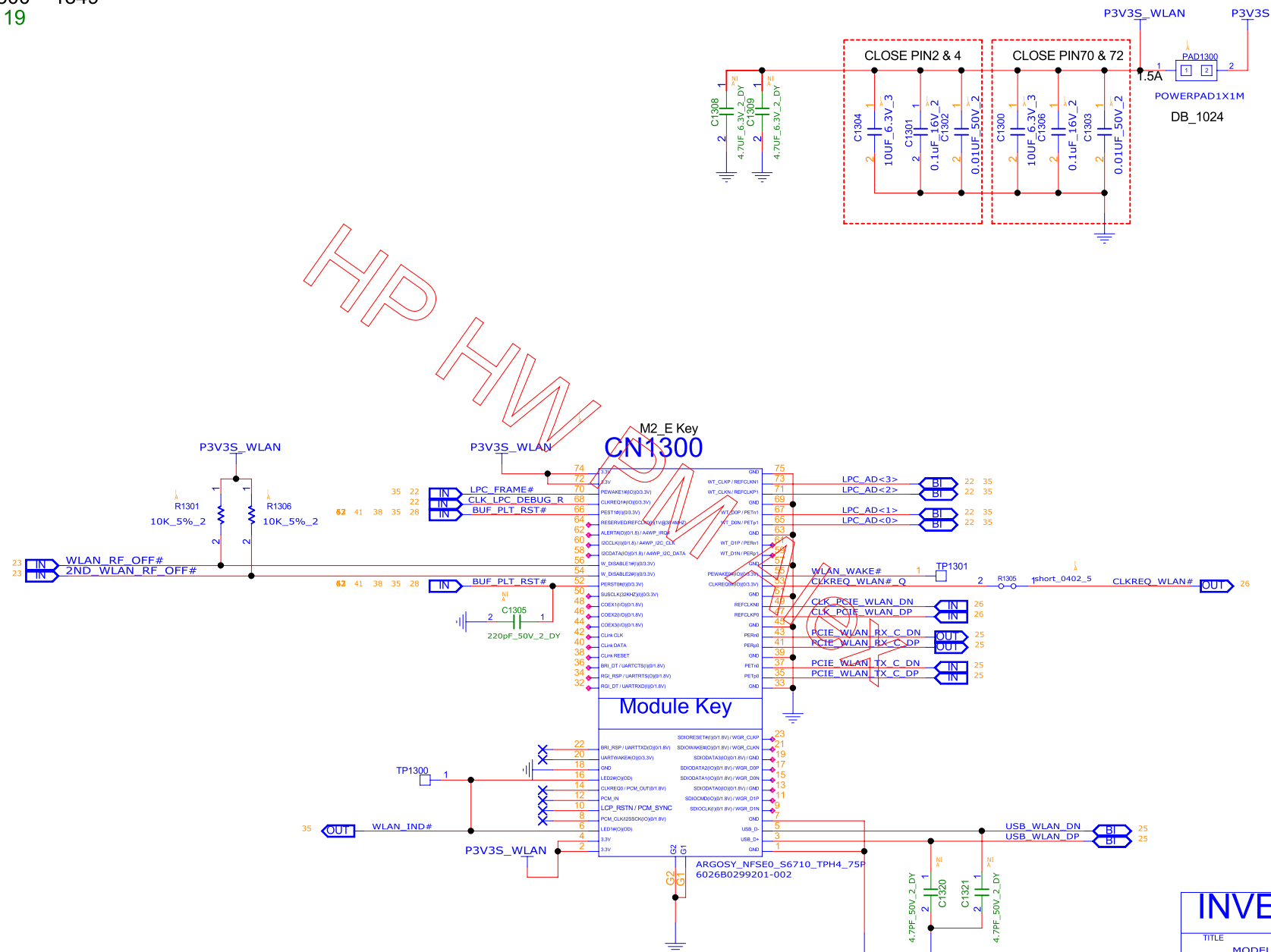
Eletro-XTechnical

WLAN

REFERENCE 1300 ~ 1349

VER.07_20171119

Eletro-XTechnical



INVENTEC

TITLE MODEL_PROJECT,FUNCTION

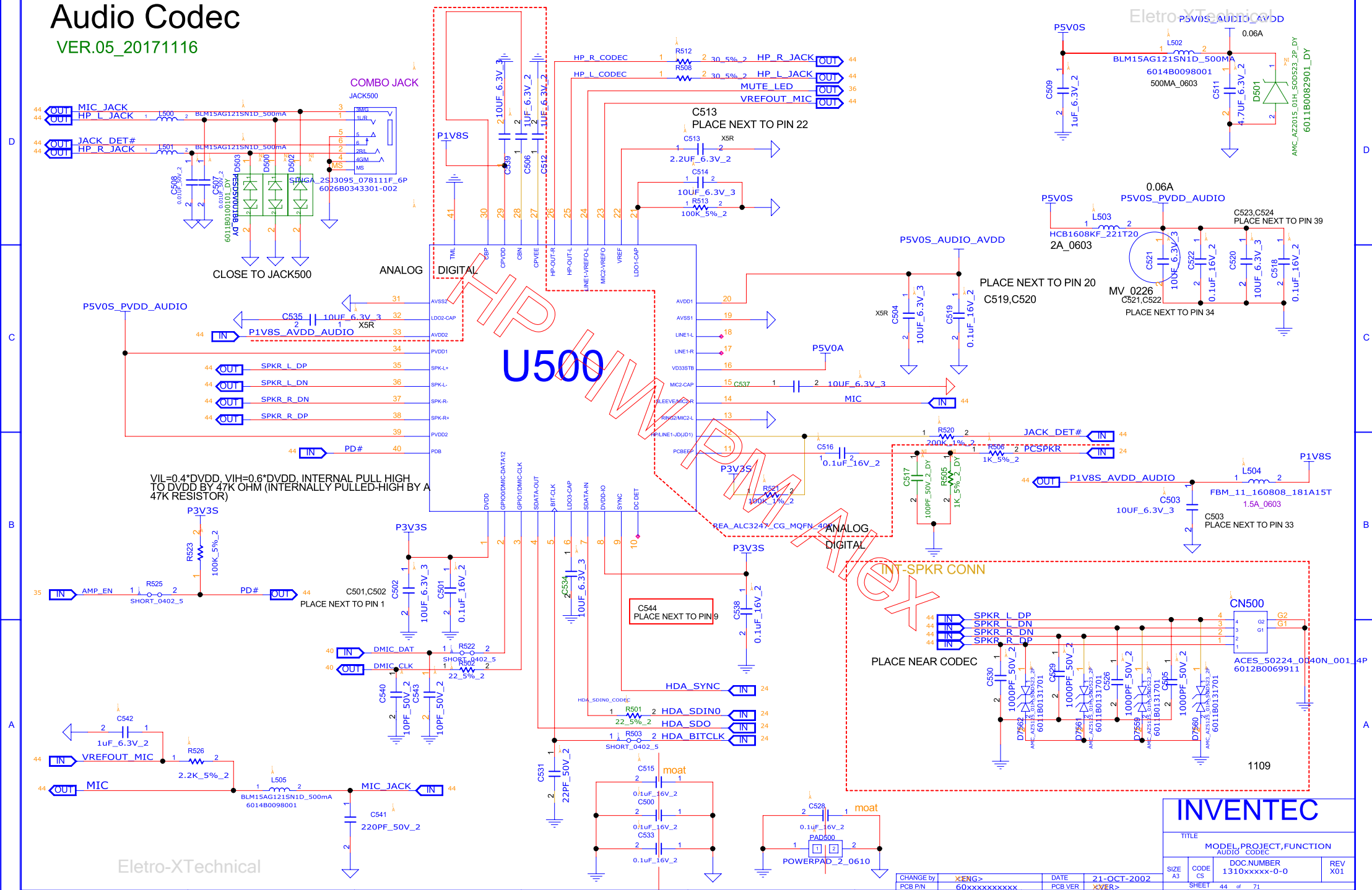
SIZE 3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

SHEET of 43 71

CHANGE by XXX PCB P/N 6026B0299201-002 DATE PCB VER X01

Eletro-XTechnical

VER.05_20171116



LAN (Transformer & RJ45)

Location 470 ~ 499

VER.05_20171107

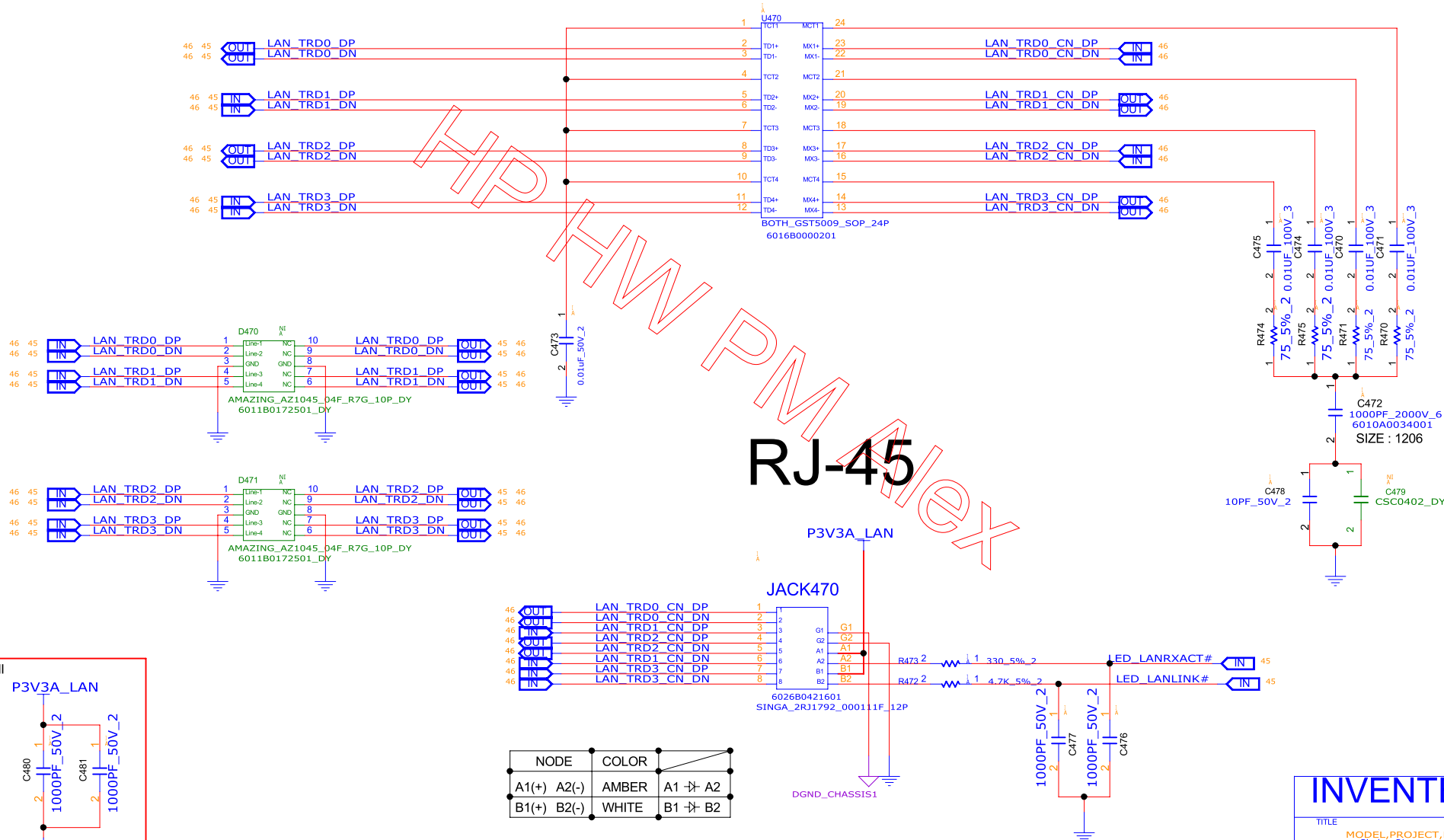
Eletro-XTechnical

For 10/100 /1000 LAN

GIGA main BOM change to 6016B0000201

10/100/1000 Main====> Bothhand P/N : 6016B0000201 GST5000

10/100/1000 2nd====> LANKom P/N : 6016B0003202 LG-2413S-1



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION

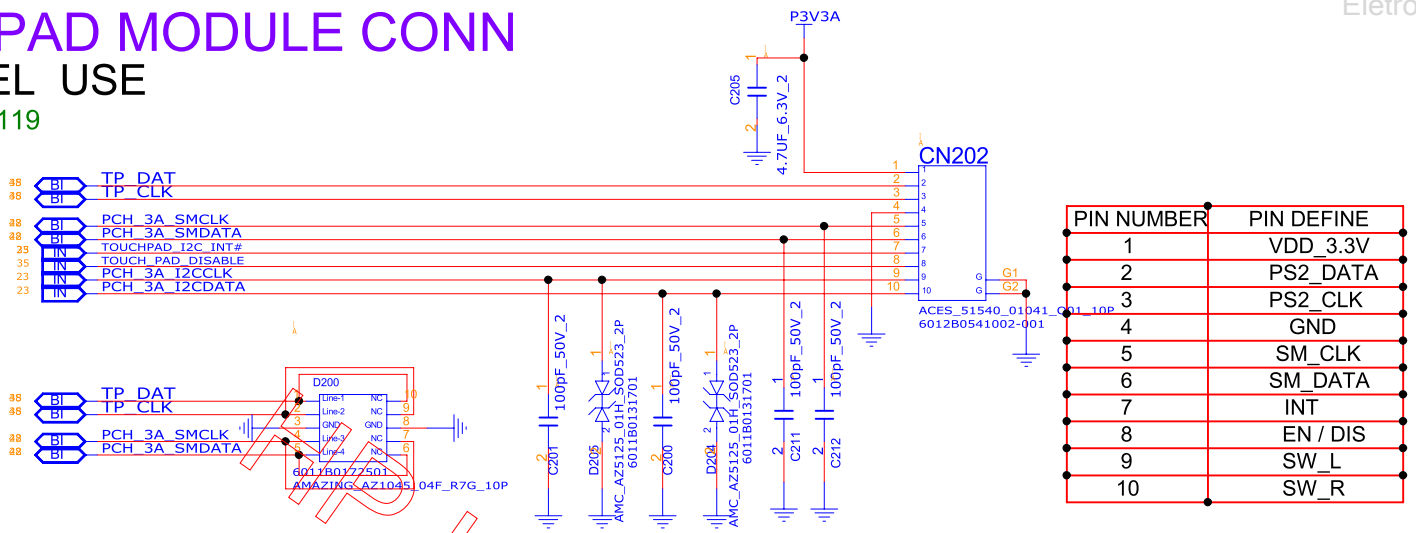
SIZE CODE DOC NUMBER REV
A3 CS 1310xxxxx-0-0 X01

CHANGE by XXX
PCB P/N 60xxxxxxx
DATE 21-OCT-2002
PCB VER XXX

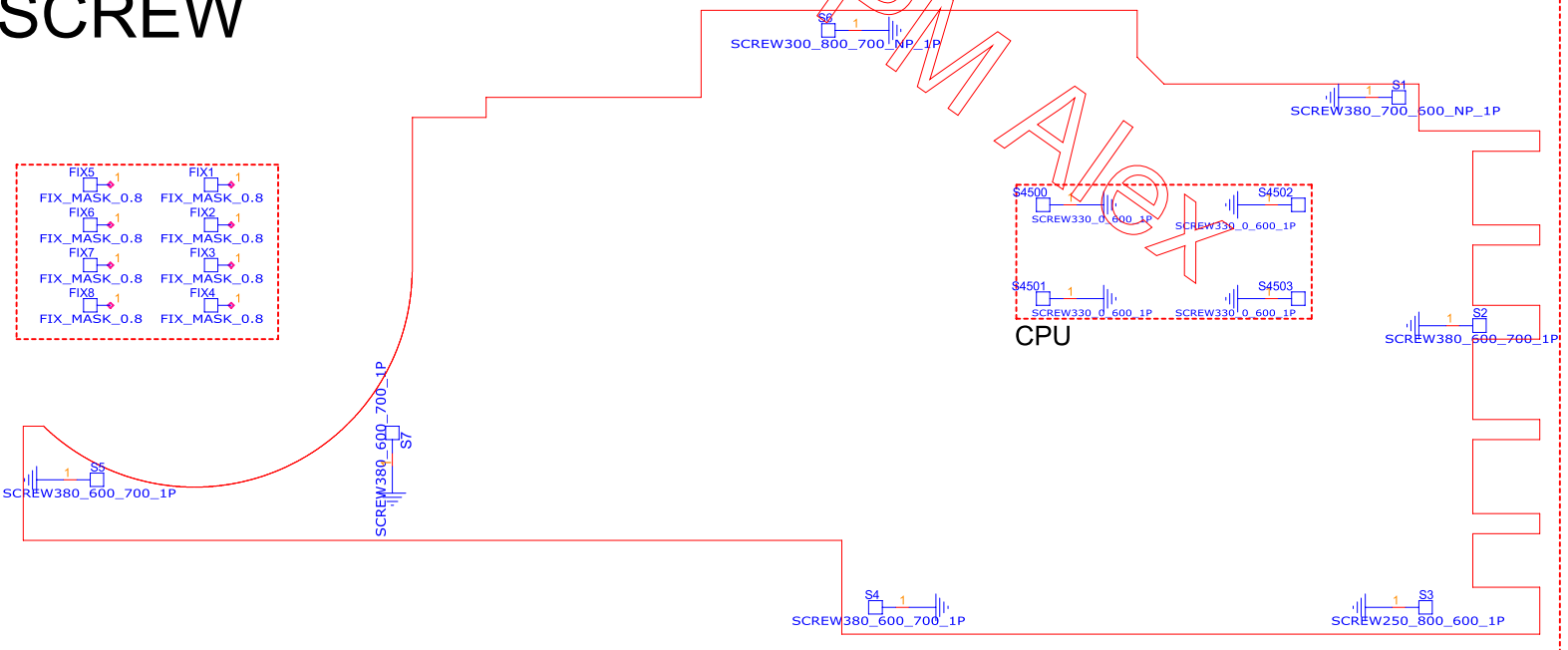
SHEET 46 of 71

TOUCHPAD MODULE CONN
FOR INTEL USE
VER.14_20171119

Eletro-XTechnical



SCREW



INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
POWER BUTTON			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		of 48	71

CHANGE by	DATE
PCB P/N	PCB VER
XXX	XXX
601280541002-001	XXX

Eletro-XTechnical

VER.12_20171120

Eletro-XTechnical



TITLE	MODEL,PROJECT,FUNCTION
	Block Diagram

SIZE	CODE	DOC NUMBER
------	------	------------

A3	CS	1310xxxxx-0-0
----	----	---------------

	SHEET	49	d	71
			1	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

SIZE A3	CODE C5	DOC NUMBER 1310xxxxxx-0-0	REV X01
SHEET 49 of 71			



Small Board

- 1.USB & CR FOR NARROW BORDER (LOCATION : 9200)
- 2.USB & CR FOR STANDARD BORDER (LOCATION : 9600)
- 3. PICK BUTTON BOARD (LOCATION : 9300)

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	C5	1310XXXX-0-0	X01
SHEET 50 of 71			

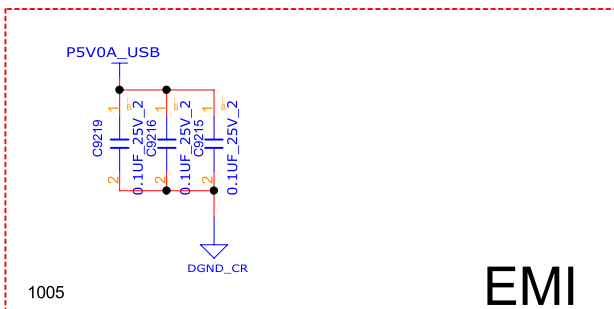
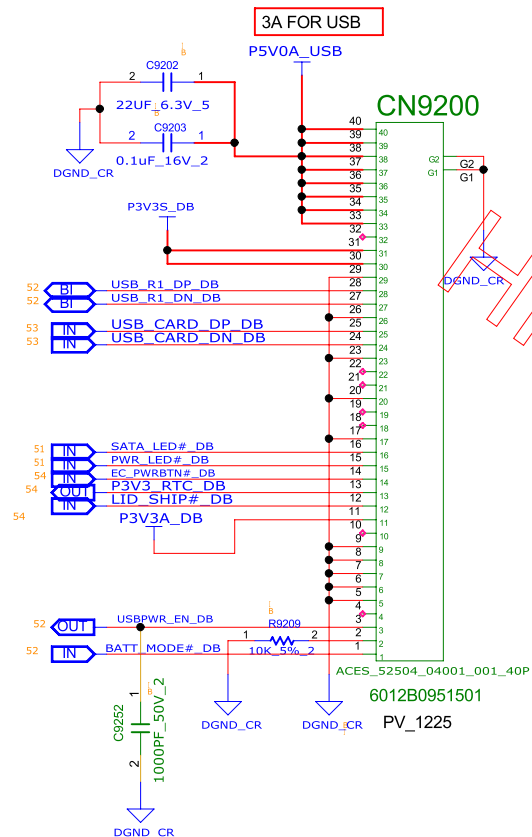
CHANGE by	XXX	DATE	21-OCT-2002
PCB PIN	60XXXXXXXXXX	PCB VER	XXX

CARDREADER USB BOARD

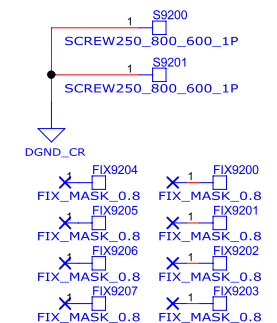
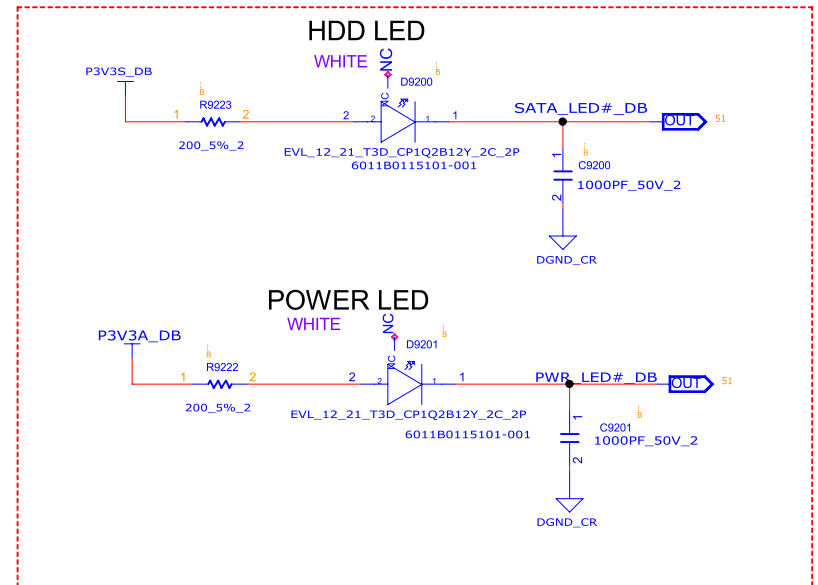
FOR STANDER BORDER USE

VER.10_20171109

Eletro-XTechnical



EMI



INVENTEC

TITLE MODEL,PROJECT,FUNCTION

SIZE CODE DOC NUMBER REV

A3 CS 1310xxxxx-0-0 X01

SHEET of 51 71

CHANGE by XXX DATE PCB VER XXXX-XXXX-XXXX

VER.10_20171109

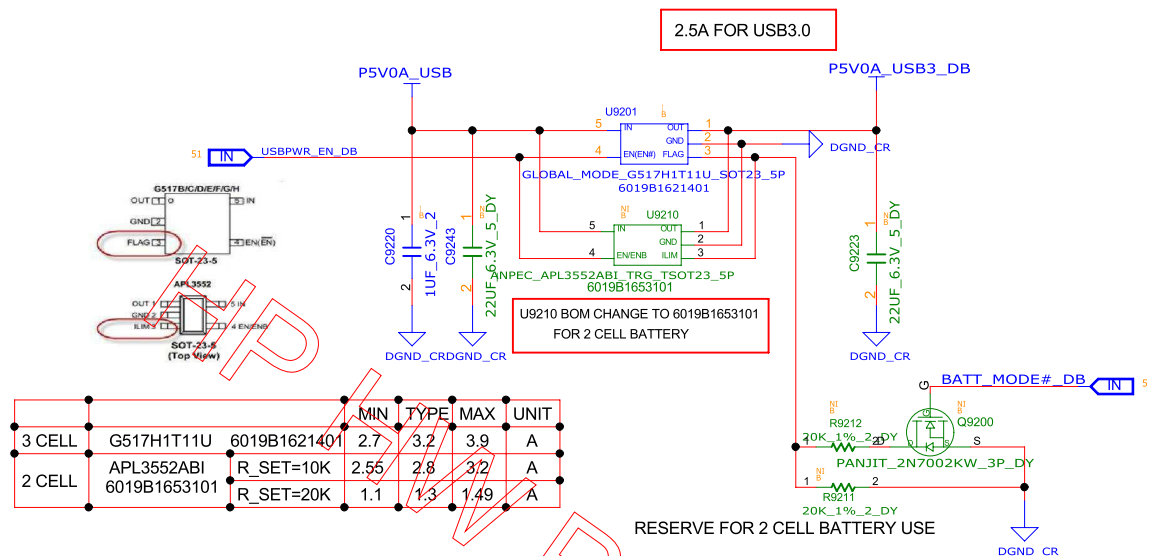
Eletro-XTechnical

USB2.0 CNTR

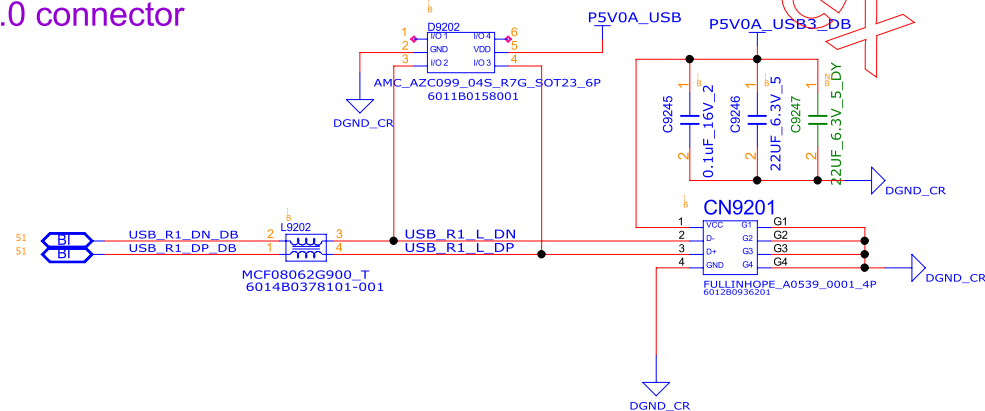
FOR STANDER BORDER USE

VER.08_20180102

Eleto-XTechnical



USB2.0 connector



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION
	CRT_CONN

SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET 52 of 71			

CHANGE by	XENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XVER>

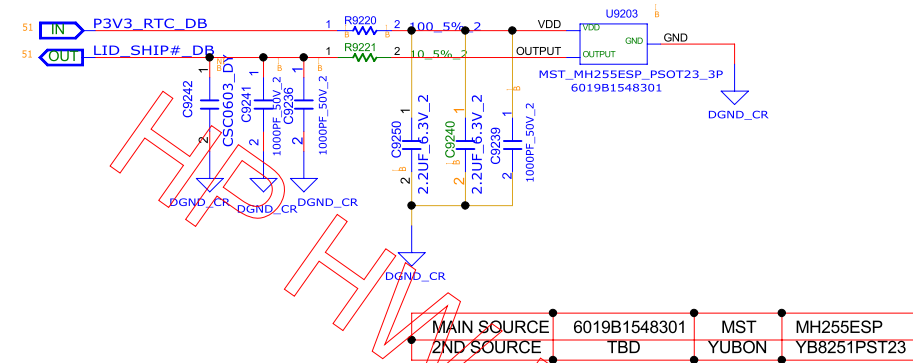
POWER BUTTON & LID

FOR STANDER BORDER USE

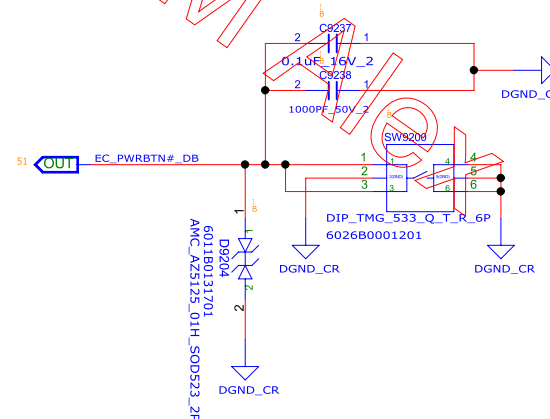
VER.09_20171120

LID SW

0.005 mA



POWER BUTTON



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3
CODE CS
DOC NUMBER 1310xxxxx-0-0
REV X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX

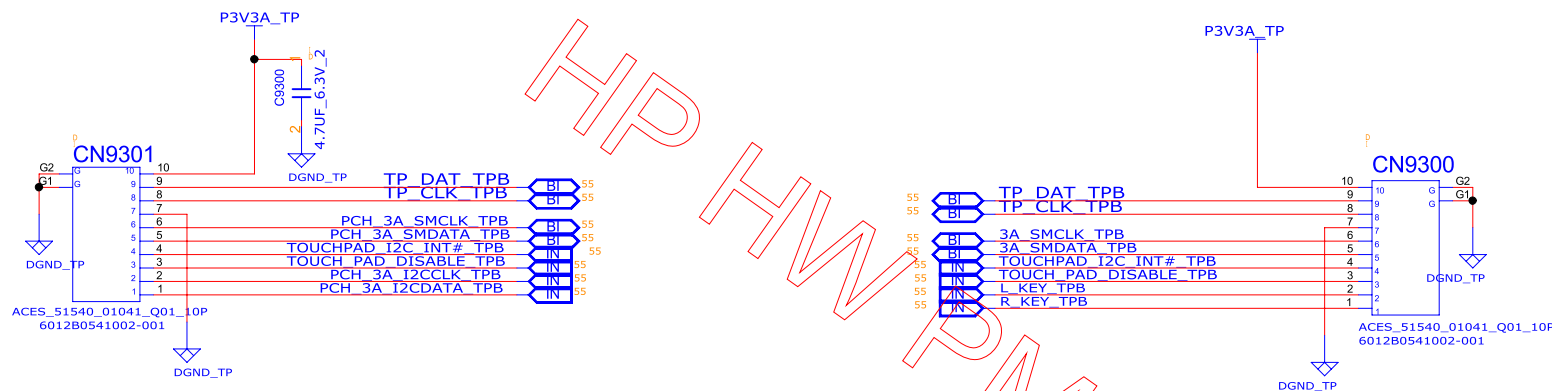
SHEET 54 of 71

PICK BUTTON (TYPE_A)

TOUCHPAD R / L BOARD

VER.14_20171119

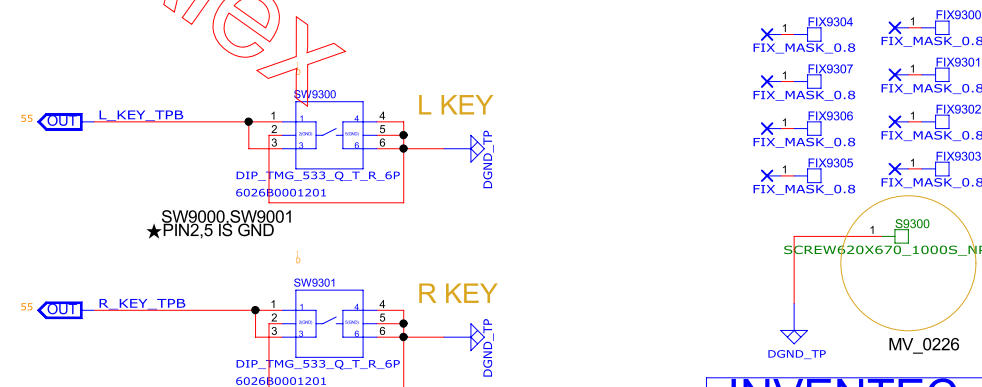
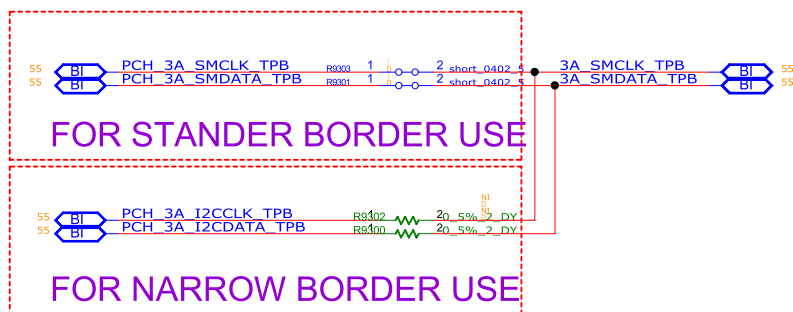
Eletro-XTechnical



PIN DEFINE	PIN NUMBER
VDD_3.3V	1
PS2_DATA	2
PS2_CLK	3
GND	4
SM_CLK	5
SM_DATA	6
INT	7
EN / DIS	8
SW_L	9
SW_R	10

TO MAIN BOARD

TO TP MODULE



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 55 of 71			

CHANGE by	X-ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	X-VER>

Eletro-XTechnical

AMD R17M-30/70

GDDR5 4PCSX16

2017.10.23

R17M-M1-30/70 BOOT VID
BOOT VID CODE

SVC	SVD	VOLTAGE SELECTED(V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

R17M-M1-30/70 SVI2 LEVEL SHIFT OPTION TABLE

R17M-M1 30(3.3V)
R17M-M1 30 SVI2 PATH

ATI_R17	R5216	R5217	R5220	R5219	R5218	R5225	R5226	R5221
M1-70	DY	DY	DY	DY	DY	DY	DY	DY
M1-30	STUFF	STUFF	DY	STUFF	STUFF	STUFF	STUFF	DY

R17M-M1 70(1.8V)
R17M-M1 70 SVI2 PATH

ATI_R17	R5100	R5101	R5102	R5103	R5104	R5105
M1-70	DY	DY	STUFF	DY	STUFF	DY
M1-30	DY	DY	DY	DY	DY	DY

R17M-M1 30(3.3V)
R17M-M1 70(1.8V) VR VDDIO SETTING

ATI_R17	R67022	R67024
M1-70	DY	STUFF
M1-30	STUFF	DY

R17M-M1-30/70 MLPS OPTION TABLE

ATI_R17	R5051	R5050
M1-70	DY	DY
M1-30	DY	STUFF

R17M-M1-30/70 PART NUMBER TABLE

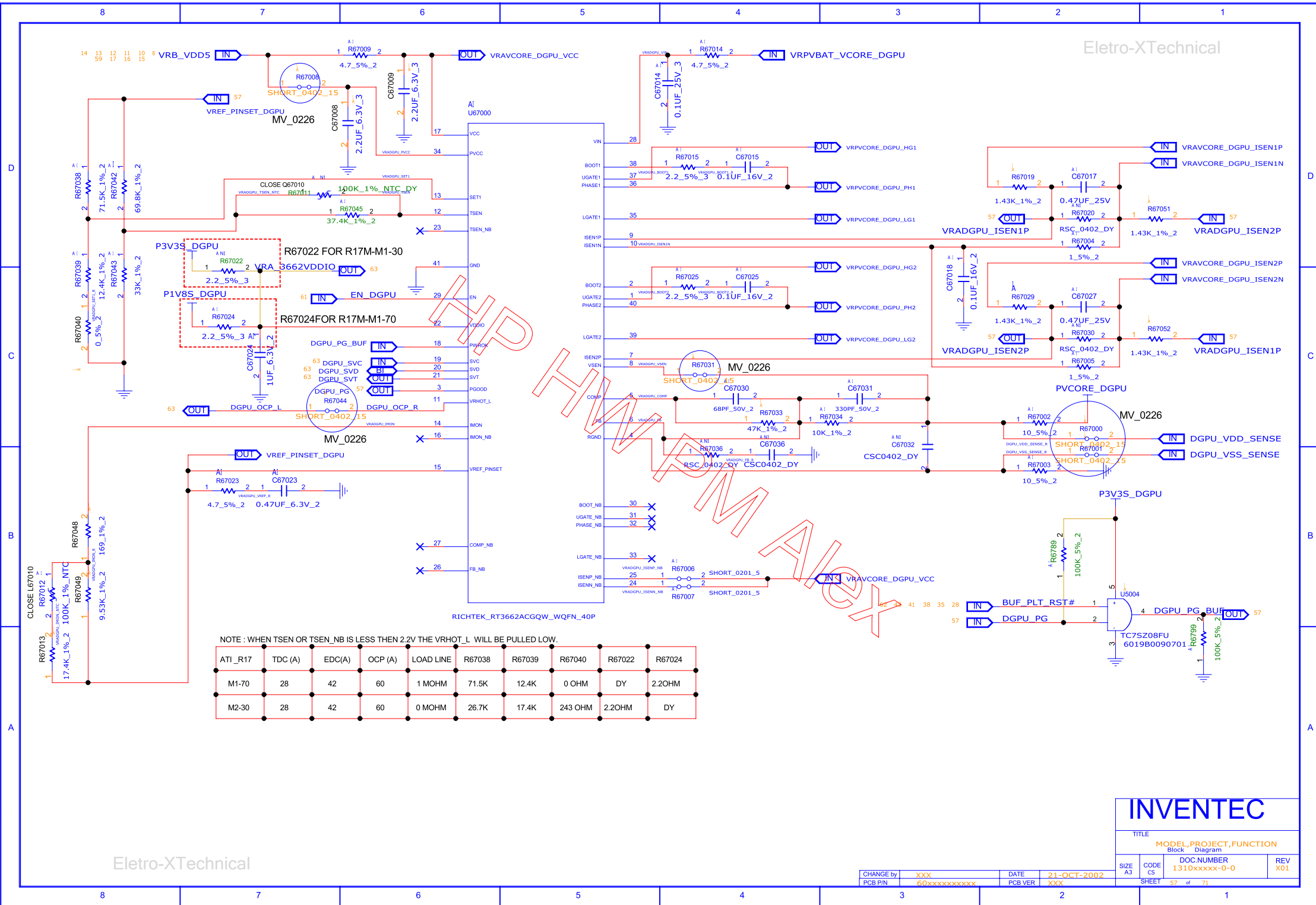
ATI_R17	U5000
M1-70	6019B1639501
M1-30	6019B1639401

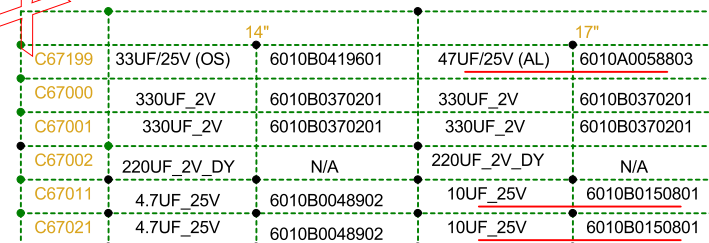
R17M-M1-30/70 LOAD LINE OPTION TABLE

ATI_R17	R5213	R5212
M1-70	0 OHM	0 OHM
M1-30	DY	DY

R17M-M1-30/70 VCORE POWER OPTION TABLE

ATI_R17	R5202	R5206
M1-70	0 OHM	0 OHM
M1-30	DY	DY



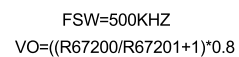


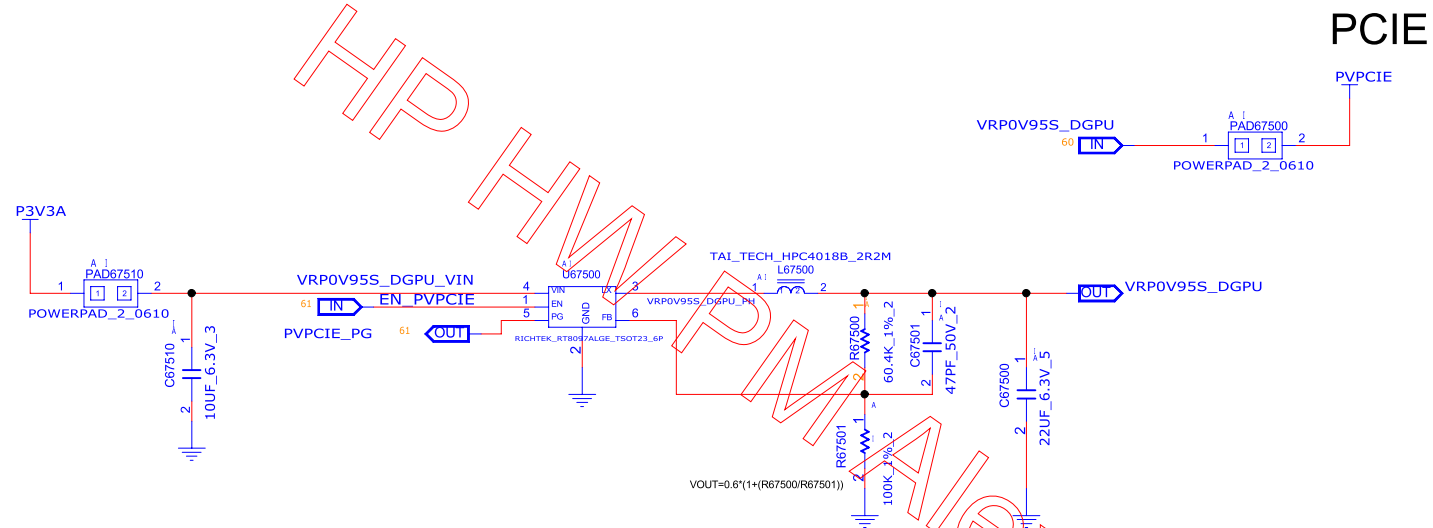
INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
Block	Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	
SHEET		58 of 71	

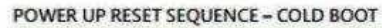
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



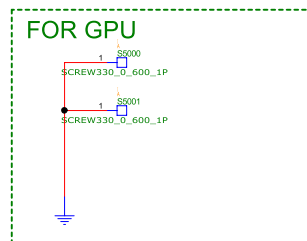
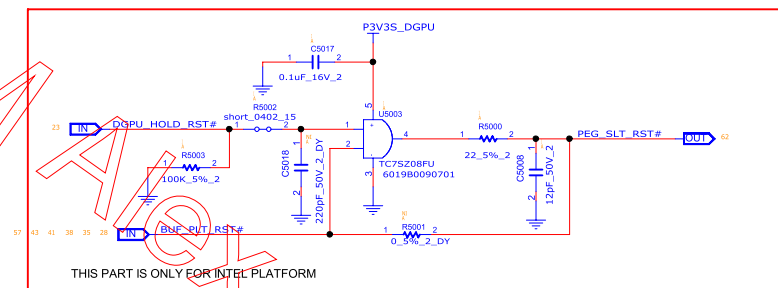
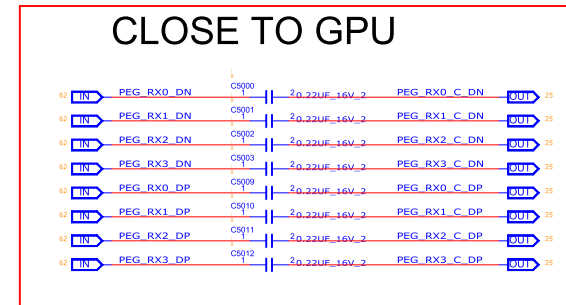
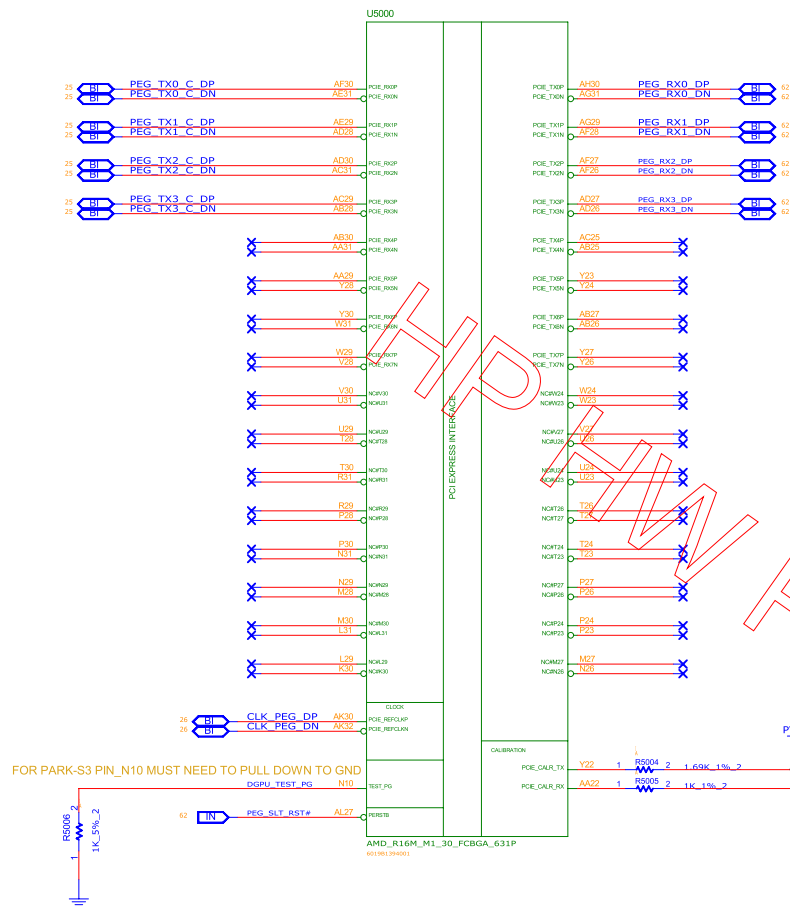


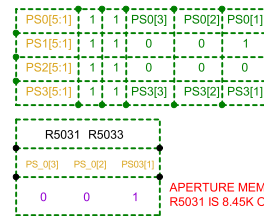
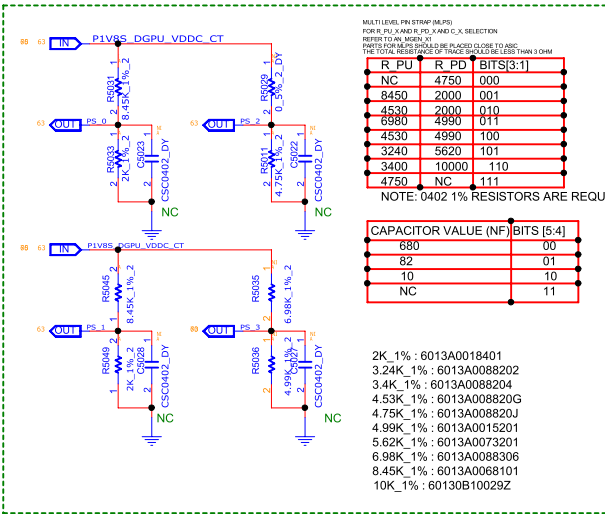
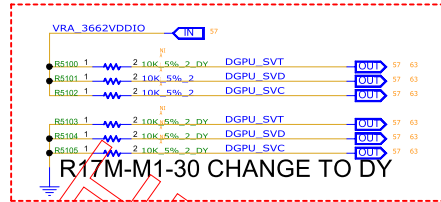
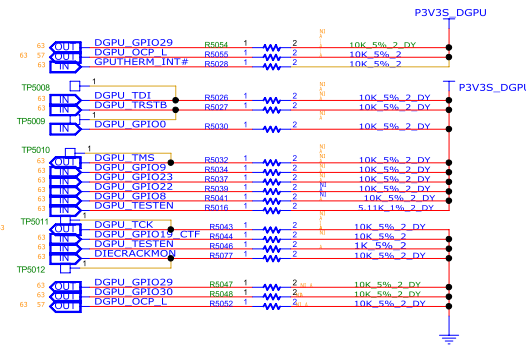
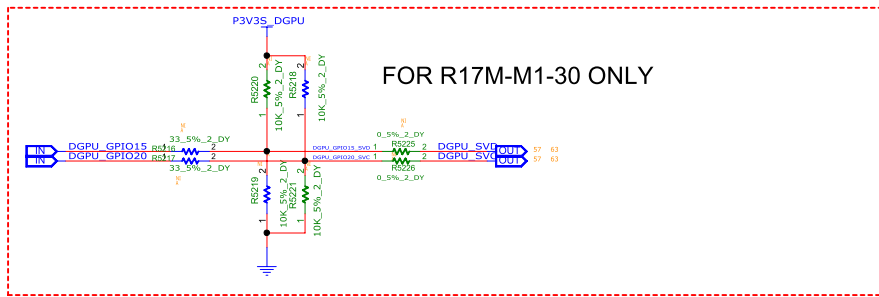
P1V8S_DGPU

POWER DOWN



TITLE				MODEL,PROJECT,FUNCTION					
				Block Diagram					
SIZE A3	CODE CS	DOCNUMBER 1310xxxxx-0-0				REV X0			
SHEET				61 of 71					





VRAM ID TABLE

R5035	R5036	PS_3[3]	PS_3[2]	PS_3[1]	VENDER	IEC PIN	CONFIGURATION	VENDER PIN
NC	4.75K	0	0	0	Hynix	6019B1542101	512M X16	H5GC8H24MJR-R0C
8.45K	2K	0	0	1	Micron	6019B1486001	512M X16	MT51J256M32HF-70A
4.53K	2K	0	1	0	Samsung	6019B1485901	512M X16	K4G80325FB-HC28
6.98K	4.99K	0	1	1			512M X16	
4.53K	4.99K	1	0	0	Hynix	6019B1542101	256M X 32	H5GC8H24MJR-R0C
3.24K	5.62K	1	0	1	Micron	6019B1486001	256M X 32	MT51J256M32HF-70A
3.4K	10K	1	1	0	Samsung	6019B1485901	256M X 32	K4G80325FB-HC28
4.75K	NC	1	1	1			256M X 32	

FOUR PIECES CHIP

FOUR PIECES CHIP

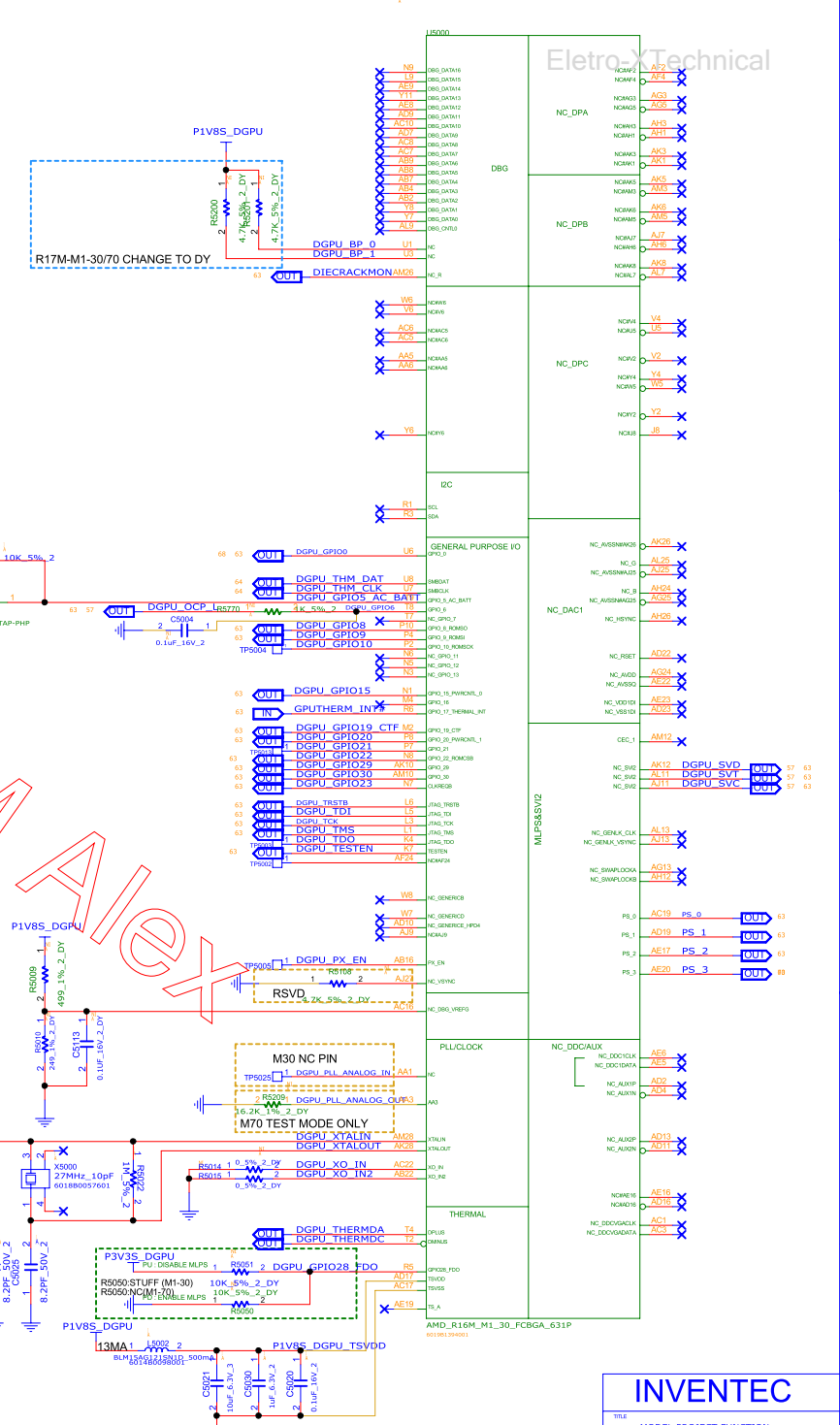
FOUR PIECES CHIP

FOUR PIECES CHIP

TWO PIECES CHIP

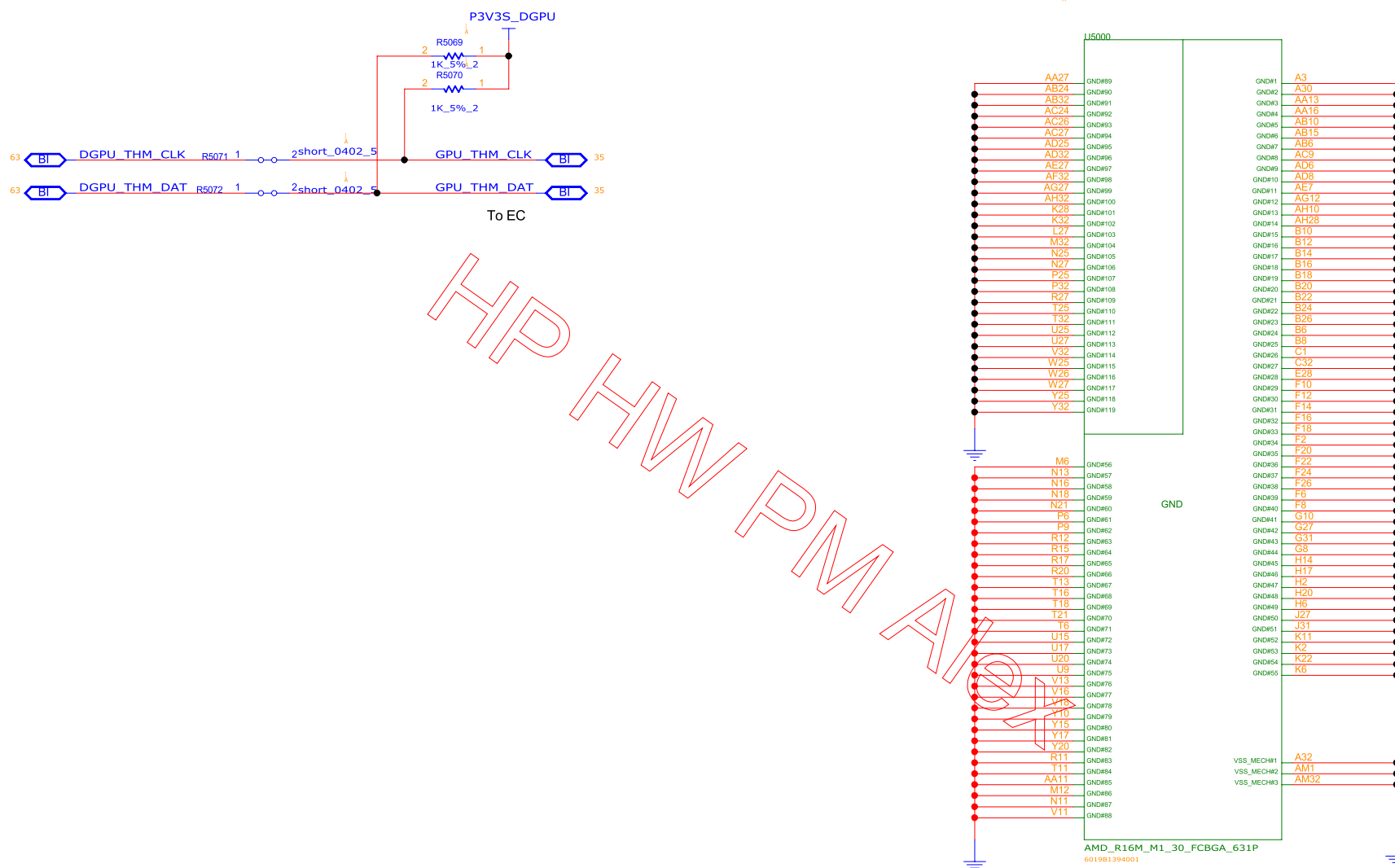
TWO PIECES CHIP

TWO PIECES CHIP



Eleto-XTechnical

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX





SIZE A3	CODE CS	1310xxxxx-0-0	
SHEET		1 of 55	34

CHANGE by	XXX	DATE	
PCB P/N	60MCXXXXXXXX	PCB VER	XVER OCT-2002



Eleto-XTechnical

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
SEYMOUR XT-S3

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		62 of 71	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

MEMORY: FBA Partition 31..0

U5501

NORMAL

BYTE-1

BYTE-3

P1V55_DGPU

X16 MODE=GND

1 R5507 2

60.4 1% 2

1 R5508 2

60.4 1% 2

1 R5509 2

60.4 1% 2

1 R5510 2

60.4 1% 2

1 R5511 2

60.4 1% 2

1 R5512 2

60.4 1% 2

1 R5513 2

60.4 1% 2

1 R5514 2

60.4 1% 2

1 R5515 2

60.4 1% 2

1 R5516 2

60.4 1% 2

1 R5517 2

60.4 1% 2

1 R5518 2

60.4 1% 2

1 R5519 2

60.4 1% 2

1 R5520 2

60.4 1% 2

1 R5521 2

60.4 1% 2

1 R5522 2

60.4 1% 2

1 R5523 2

60.4 1% 2

1 R5524 2

60.4 1% 2

1 R5525 2

60.4 1% 2

1 R5526 2

60.4 1% 2

1 R5527 2

60.4 1% 2

6019B1281401

P1V55_DGPU

U5501

U5501

U5501

U5501

U5501

U5501

U5501

U5501

U5501

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U5501

U5501

U5501

U5501

U5501

U5500

MIRROR

BYTE-2

BYTE-0

P1V55_DGPU

X16 MODE=GND

1 R5507 2

60.4 1% 2

1 R5508 2

60.4 1% 2

1 R5509 2

60.4 1% 2

1 R5510 2

60.4 1% 2

1 R5511 2

60.4 1% 2

1 R5512 2

60.4 1% 2

1 R5513 2

60.4 1% 2

1 R5514 2

60.4 1% 2

1 R5515 2

60.4 1% 2

1 R5516 2

60.4 1% 2

1 R5517 2

60.4 1% 2

1 R5518 2

60.4 1% 2

1 R5519 2

60.4 1% 2

1 R5520 2

60.4 1% 2

1 R5521 2

60.4 1% 2

1 R5522 2

60.4 1% 2

1 R5523 2

60.4 1% 2

1 R5524 2

60.4 1% 2

1 R5525 2

60.4 1% 2

1 R5526 2

60.4 1% 2

1 R5527 2

60.4 1% 2

6019B1281401

P1V55_DGPU

U5500

U5500

U5500

U5500

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INVENTEC

MODEL/PROJECT/FUNCTION

Block Diagram

SIZE CODE DOC NUMBER REV

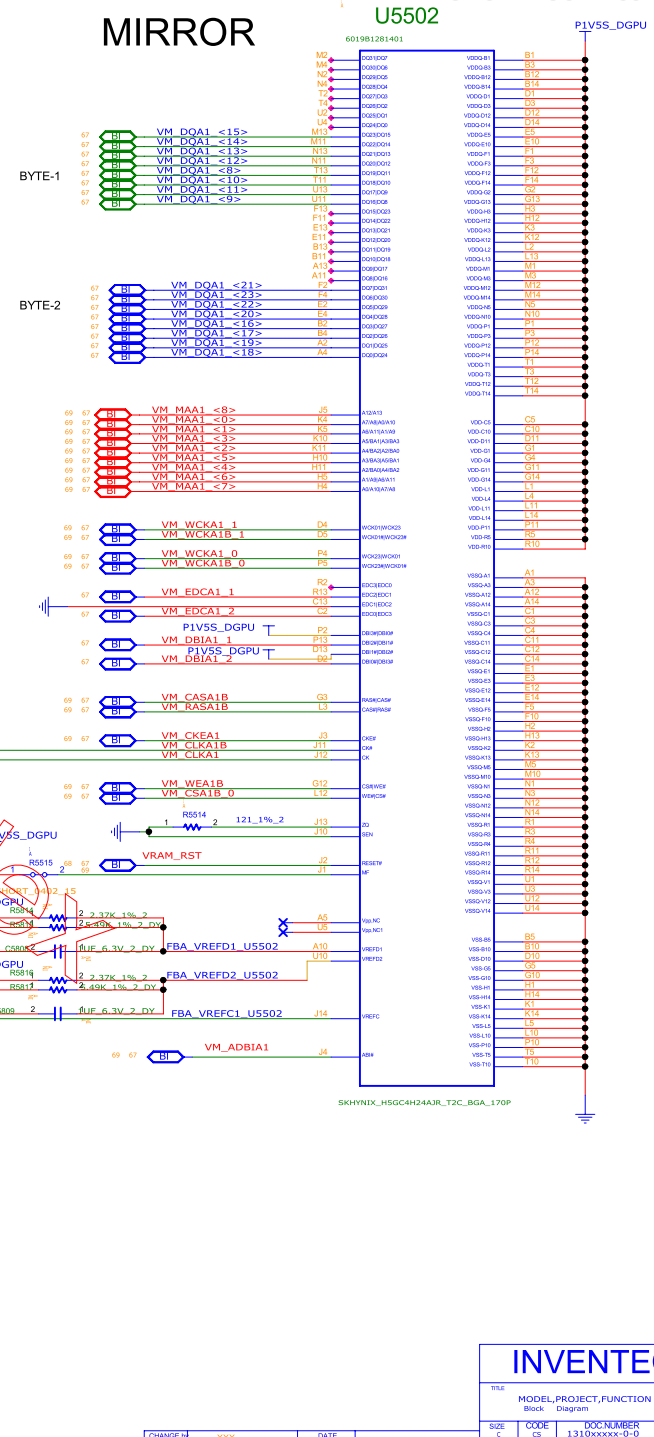
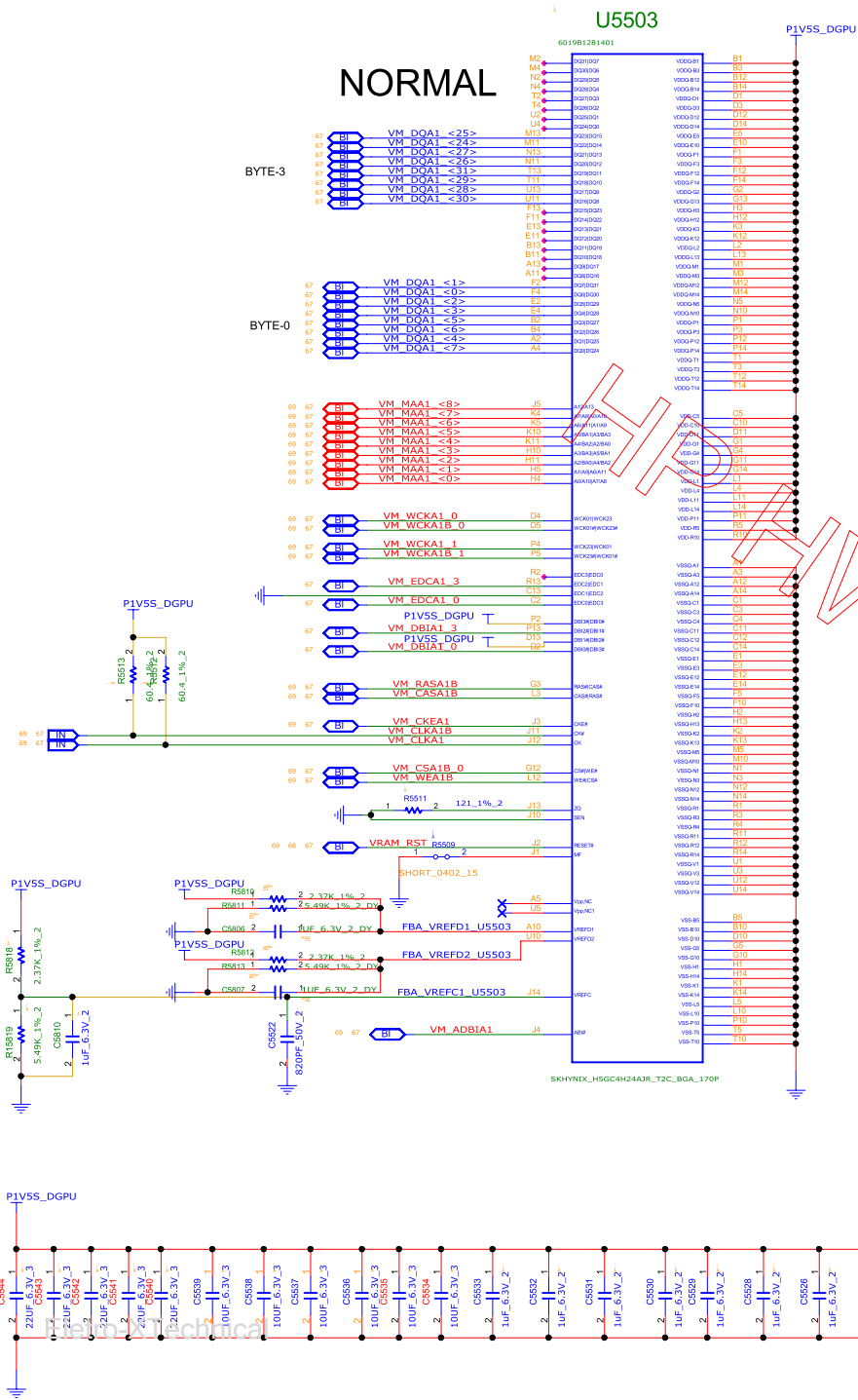
SHEET 1 11

CHANGE PCB PIN

DATE PCB VER 2

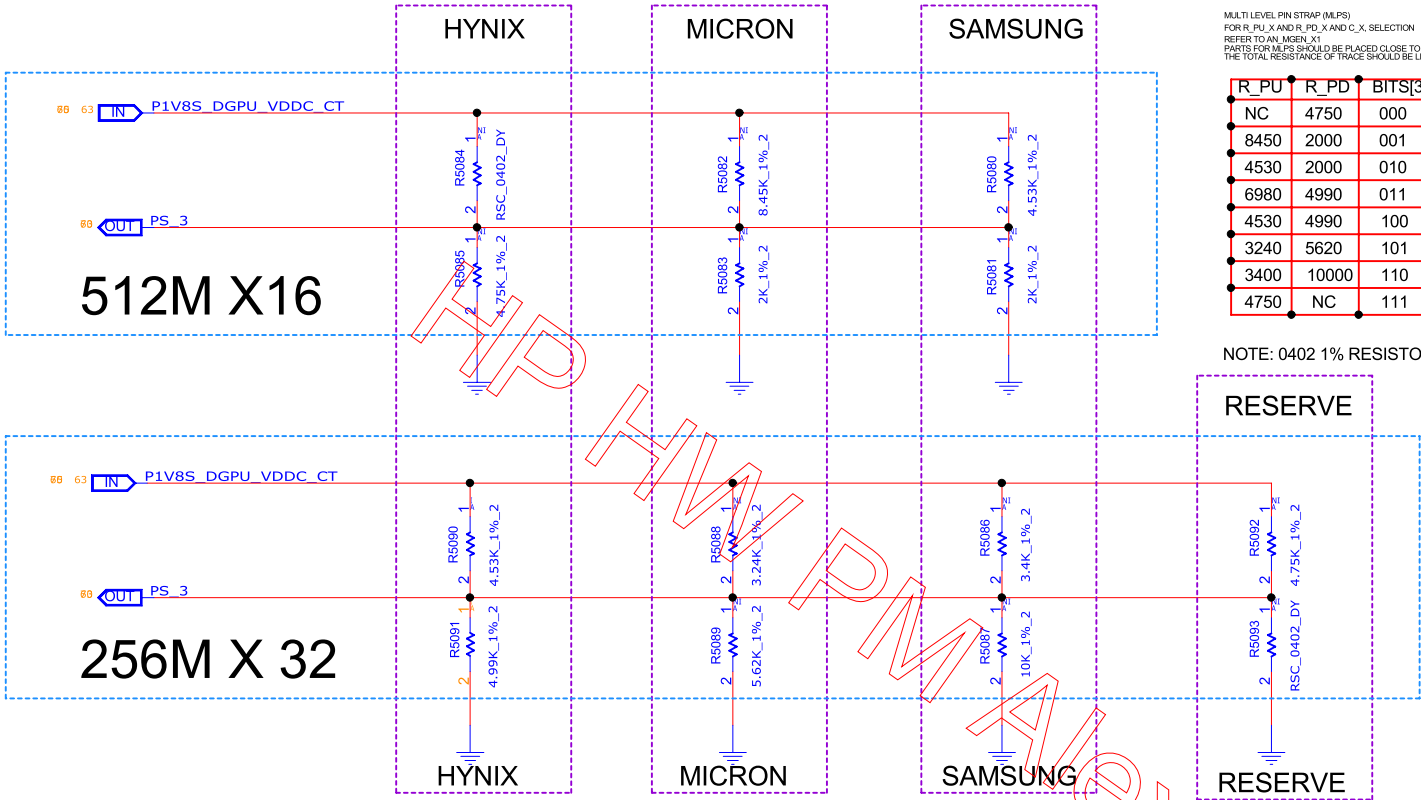
DATE PCB VER 2

DATE PCB VER 2



VRAM ID

Eletro-XTechnical



MULTI LEVEL PIN STRAP (MLPS)
FOR R_PU, X AND R_PD, X AND C_X, SELECTION
REFER TO AN M0EN X1
PARTS FOR MLPS SHOULD BE PLACED CLOSE TO ASIC
THE TOTAL RESISTANCE OF TRACE SHOULD BE LESS THAN 3 OHM

R_PU	R_PD	BITS[3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

2K_1% : 6013A0018401
3.24K_1% : 6013A0088202
3.4K_1% : 6013A0088204
4.53K_1% : 6013A008820G
4.75K_1% : 6013A008820J
4.99K_1% : 6013A0015201
5.62K_1% : 6013A0073201
6.98K_1% : 6013A0088306
8.45K_1% : 6013A0068101
10K_1% : 60130B10029Z

NOTE: 0402 1% RESISTORS ARE REQUIRED.

VRAM ID TABLE

R_PU	R_PD	PS_3[3]	PS_3[2]	PS_3[1]	VENDER	IEC P/N	CONFIGURATION	VENDER P/N
NC (R5084)	4.75K (R5085)	0	0	0	Hynix	6019B1542101	512M X16	H5GC8H24MJR-R0C
8.45K (R5082)	2K (R5083)	0	0	1	Micron	6019B1486001	512M X16	MT51J256M32HF-70:A
4.53K (5080)	2K (R5081)	0	1	0	Samsung	6019B1485901	512M X16	K4G80325FB-HC28
6.98K (R5092)	4.99K (R5093)	0	1	1	RESERVE		512M X16	
4.53K (R5090)	4.99K (R5091)	1	0	0	Hynix	6019B1542101	256M X 32	H5GC8H24MJR-R0C
3.24K (R5088)	5.62K (R5089)	1	0	1	Micron	6019B1486001	256M X 32	MT51J256M32HF-70:A
3.4K (R5086)	10K (R5087)	1	1	0	Samsung	6019B1485901	256M X 32	K4G80325FB-HC28
4.75K (R5092)	NC (R5093)	1	1	1	RESERVE		256M X 32	

FOUR PIECES CHIP
FOUR PIECES CHIP
FOUR PIECES CHIP
FOUR PIECES CHIP
TWO PIECES CHIP
TWO PIECES CHIP
TWO PIECES CHIP
TWO PIECES CHIP

INVENTEC

TITLE MODEL,PROJECT,FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

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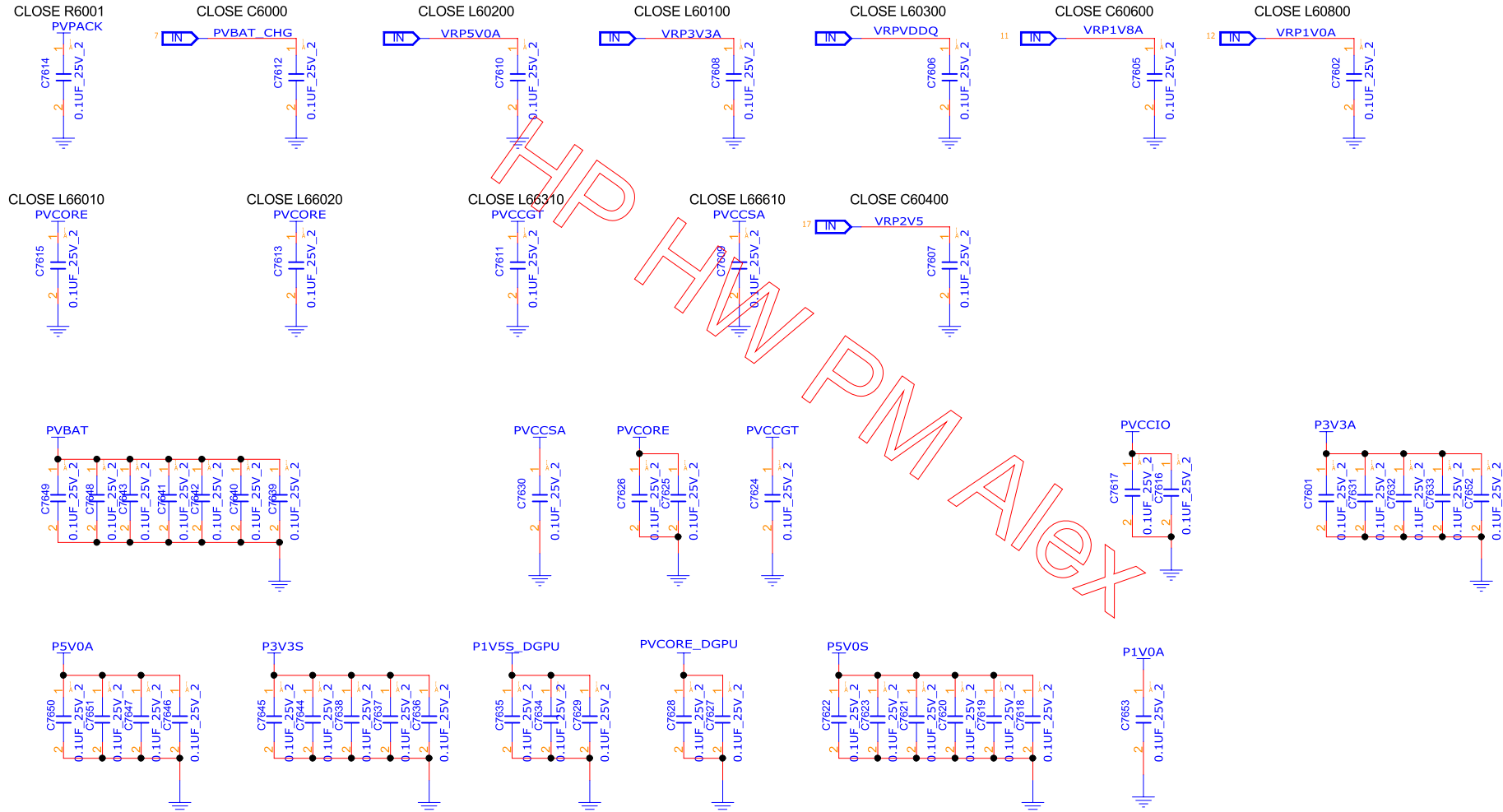
CHANGE by XXX PCB P/N 60xxxxxxxxxxx DATE 21-OCT-2002 PCB VER XXX

Eletro-XTechnical

EMI SOLUTION

LOCATION : 7600 - 7699

Eletro-XTechnical



Eletro-XTechnical

INVENTECTITLE
MODEL, PROJECT, FUNCTION

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by	DATE
PCB P/N XXX	21-OCT-2002
PCB VER 60xxxxxxxxxx	XXX

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